CM4000 CENTRAL/REMOTE TEST SET

TECHNICAL MANUAL

AS4802AA

ENGINEERED SYSTEMS INC.
Phoenix, Arizona

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TECHNICAL MANUAL

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ENGINEERED SYSTEMS, INC.
1841 EAST 3RD STREET
TEMPE, ARIZONA 85281

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Most Central Stations and some Remote Stations require connection to 120-volt ac power. Be extremely careful when making these connections. Serious injury and possible fatality can result from electrical shock.

CENTRAL/REMOTE TEST SET

CM4141M-1

OPERATIONS MANUAL

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1. GENERAL

THE CM4141M-1 TEST SET IS A FIELD SERVICE TOOL USED TO TEST CM4000 CENTRAL AND REMOTE STATIONS. SALIENT FEATURES INCLUDE:

**ENCODING OF SWITCH DERIVED DATA INTO SERIALLY STRUCTURED DIGITAL MESSAGES WHICH ARE TRANSMITTED AS FREQUENCY SHIFT KEYED (FSK) AUDIO SIGNALS.

**DECODING OF SERIALLY STRUCTURED DIGITAL MESSAGES RECEIVED AS FSK AUDIO SIGNALS AND PROCESSING THEM FOR OPERATOR VIEWING.

**SELECTION OF FSK AUDIO FREQUENCIES TO PERMIT TESTING OF EITHER CENTRAL OR REMOTE STATIONS.

1.1 CM4000 MESSAGE STRUCTURE

THE CM4000 MESSAGE STRUCTURE CONSISTS OF CHARACTER PAIRS CALLED FRAMES. THE TOTAL NUMBER OF FRAMES REQUIRED FOR INFORMATION TRANSFER CONSTITUTES A MESSAGE.

EACH CHARACTER IN THE MESSAGE STRUCTURE CONSISTS OF A SYNCHRONIZING BIT, EIGHT INFORMATION BITS AND A STOP INTERVAL (TELETYPE CHARACTER).

FOR TRANSMISSION RATES OF 110 BAUD (10 CHARACTERS PER SECOND) OR LESS THE STOP INTERVAL IS TWO BITS IN DURATION (11 UNIT CODE).

FOR TRANSMISSION RATES GREATER THAN 110 BAUD, THE STOP INTERVAL IS (TYPICALLY) OF ONE BIT DURATION (10 UNIT CODE).

THE FIRST FRAME, CALLED THE PREFIX, IS ALWAYS A NULL CHARACTER (INFORMATION BITS ARE ZERO) FOLLOWED BY A RUBOUT CHARACTER (INFORMATION BITS ARE ONES).

SUBSEQUENT FRAMES CONSIST OF TWO IDENTICAL CHARACTERS PERMITTING BIT-BY-BIT VERIFICATION OF INFORMATION CONTENT.

NOTE SHOULD BE MADE THAT MESSAGE LENGTHS MAY VARY DEPENDENT UPON INFORMATION CONTENT.

MESSAGE LENGTHS AND INFORMATION CONTENT VARY WIDELY BETWEEN SYSTEMS THE TEST SET USER MUST REFER TO SYSTEM DOCUMENTATION FOR MESSAGE SPECIFICS RELATIVE TO HIS SYSTEM.

1.2 CONTROL/DISPLAY PANEL

THE TEST SET PANEL IS DIVIDED INTO THREE SECTIONS:

**THE LEFT SECTION RELATES TO TRANSMITTED MESSAGES

**THE CENTER SECTION RELATES, IN GENERAL, TO RECEIVED MESSAGES

**THE RIGHT SECTION RELATES TO THE TEST SET INTERFACE, POWER, ETC.

1.2.1 TRANSMIT SECTION

CONTROLS IN THE TRANSMIT AND RECEIVE SECTION PERMIT THE OPERATOR TO ESTABLISH:

- **THE INFORMATION CONTENT FOR ANY TRANSMIT MESSAGE FRAME EXCEPT THE PREFIX FRAME.

- **THE NUMBER OF FRAMES CONSTITUTING A TRANSMITTED MESSAGE.

DISPLAYS IN THE TRANSMIT SECTION PERMIT THE OPERATOR TO VIEW:

- **THE INFORMATION CONTENT OF ANY TRANSMIT MESSAGE FRAME EXCEPT THE PREFIX FRAME BY EIGHT (8), IN-LINE, LED (LIGHT EMITING DIODE) INDICATORS.

- **THE DYNAMIC STATUS OF THE TRANSMITTED CARRIER AND DATA KEYING SIGNALS ANNUNCIATED BY TWO LED INDICATORS.

1.2.2 RECEIVE SECTION

DISPLAYS IN THE RECEIVE SECTION PERMIT THE OPERATOR TO VIEW:

- **THE INFORMATION CONTENT OF ANY RECEIVED MESSAGE FRAME INCLUDING THE PREFIX FRAME AS ANNUNCIATED BY EIGHT, (8) IN-LINE LED INDICATORS.

- **THE INFORMATION CONTENT OF TWO SUCCESSIVE RECEIVED FRAMES INCLUDING THE PREFIX FRAME AS ANNUNCIATED BY FOUR, IN-LINE HEXADECIMAL DISPLAYS.

- **THE VALIDITY OF THE RECEIVED MESSAGE (SINGLE LED INDICATOR)

- **THE DYNAMIC STATUS OF THE RECEIVED CARRIER AND DATA KEYING SIGNALS AS ANNUNCIATED BY TWO LED INDICATORS.

IN ADDITION, MEANS ARE PROVIDED TO ALLOW THE IN-LINE HEXADECIMAL DISPLAY TO SHOW:

- **NUMBER OF FRAMES SELECTED FOR THE TRANSMITTED MESSAGE

- **THE NUMBER OF FRAMES RECEIVED.

1.2.3 INTERFACE SECTION

THE INTERFACE SECTION INCLUDES:

- **AC POWER CORD FOR CONNECTION TO 120 VAC COMMERCIAL POWER, IF AVAILABLE.
- **TERMINATIONS FOR POWERING THE TEST SET FROM 12 VDC (TYPICALLY AVAILABLE FROM THE UNIT UNDER TEST)
- **FUSES FOR THE AC LINE, 12 VDC AND 5 VDC POWER
- **INTERFACE CONNECTOR FOR CONNECTING THE THE UNIT UNDER TEST
- **PERSONALITY PLUG (CENTRAL/REMOTE MODE)
- **AUXILIARY CONNECTER FOR SPECIAL APPLICATIONS.

2.0 SET UP

**PERSONALITY PLUG

PLUG IN THE CENTRAL OR REMOTE PLUG AS APPLICABLE FOR THE UNIT UNDER TEST.

UNPLUG PLUG FOR REMOTE TESTIN
PLUG PLUG IN FOR CENTRAL TESTIN

**INTERFACE CABLE CONNECTIONS

FSK AUDIO FROM TEST SET: RED AND BLACK WIRE PAIR

FSK AUDIO TO TEST SET : GREEN AND WHITE WIRE PAIR

**POWER CONNECTIONS

WHEN AC POWER IS AVAILABLE, CONNECT THE TEST SET TO A SOURCE OF 120 VAC COMMERCIAL POWER.

WHEN AC POWER IS NOT AVAILABLE, CONNECT A 12 VDC BATTERY (SUCH AS A REMOTE STATION BATTERY) TO THE RED (+) AND BLACK (-) BINDING POSTS.

**AUDIO LEVELS

RECEIVE AND TRANSMIT AUDIO LEVELS SHOULD BE -15 DBM.

3.0 OPERATION SPECIFICS

3.1 MESSAGE TRANSMISSION

*TO INITIALIZE THE TRANSMIT BUFFER TO ALL ZEROS

1) SET AUX/HEX TOGGLE SWITCH (RX SECTION) TO HEX

2) SET FRAME SELECT THUMBWHEELS (TX SECTION) TO "00".

3) DEPRESS ENTER PUSHBUTTON (TX SECTION)

*TO ENTER CHARACTER BIT PATTERNS INTO THE TRANSMIT BUFFER

1) SET AUX/HEX TOGGLE SWITCH (RX SECTION) TO HEX

2) SET FRAME SELECT THUMBWHEEL (TX SECTION) TO APPLICABLE FRAME.

3) SET THE EIGHT TOGGLE SWITCHES (TX SECTION) TO THE BIT PATTERN DESIRED

4) DEPRESS THE ENTER PUSHBUTTON (TX SECTION)

5) NOTE THAT THE EIGHT, BIT LEDS (TX SECTION) REFLECT THE BIT PATTERN ENTERED.

6) REPEAT STEPS 2 THROUGH 5 AS DESIRED FOR EACH FRAME

*TO VIEW THE CHARACTER BIT PATTERNS IN THE TRANSMIT BUFFER

1) SET FRAME SELECT TO DESIRED FRAME

2) VIEW THE CHARACTER BIT PATTERN IN THE SELECTED FRAME AS ANNUNCIATED BY THE EIGHT, BIT LEDS (TX SECTION)

NOTE: WHEN THE FRAME SELECT THUMBWHEELS (TX SECTION) ARE SET TO "00", THE EIGHT, BIT LEDS (TX SECTION) WILL BE OFF.

THE EIGHT, BIT LEDS (TX SECTION) ARE NOT EFFECTED BY THE POSITION OF THE AUX/HEX TOGGLE SWITCH (RX SECTION).

3.1 MESSAGE TRANSMISSION (CONTINUED)

*TO SET THE NUMBER OF FRAMES CONSTITUTING A MESSAGE

1) SET AUX/HEX SWITCH (RX SECTION) TO AUX

2) SET FRAME SELECT THUMBWHEELS (TX SECTION) TO THE NUMBER OF FRAMES DESIRED IN THE MESSAGE

3) DEPRESS THE ENTRY PUSHBUTTON (TX SECTION)

4) NOTE THAT THE NUMBER OF FRAMES ENTERED IS ANNUNCIATED IN DIGITS 1 AND 2 OF THE IN-LINE DISPLAY (RX SECTION). THESE DIGITS WILL BE BLINKING.

*TO VIEW THE NUMBER OF FRAMES CONSTITUTING A TRANSMITTED MESSAGE

1) SET AUX/HEX SWITCH (RX SECTION) TO AUX

2) VIEW THE NUMBER OF FRAMES IN DIGITS 1 AND 2 OF THE IN-LINE DISPLAY (RX SECTION). THESE DIGITS WILL BE BLINKING.

*TO INITIATE A MESSAGE TRANSMISSION

1) SET THE AUTO/MANUAL TOGGLE SWITCH (TX SECTION) TO MANUAL

2) DEPRESS THE TX INITIATE PUSHBUTTON (TX SECTION)

WHEN A TRANSMISSION TAKES PLACE THE "TX ON" LAMP INDICATES CARRIER ON AND THE "TX DATA" LAMP INDICATES BINARY ONES IN THE TRANSMITTED MESSAGE.

*TO INITIATE REPETITIVE MESSAGE TRANSMISSIONS

1) SET THE AUTO/MANUAL TOGGLE SWITCH (TX SECTION) TO AUTO

MESSAGES WILL AUTOMATICALLY BE GENERATED AT APPROXIMATELY FIVE SECOND INTERVALS.

3.2 RECEIVED MESSAGES

WHEN THE PREFIX FRAME OF A MESSAGE IS RECEIVED, THE RECEIVE BUFFER IS INITIALIZED TO ALTERNATING ONES AND ZEROS.

THE VALIDITY LED WILL BE ON STEADY STATE IF ALL FRAMES OF THE RECEIVED MESSAGE ARE VALID.

WHEN A MESSAGE IS BEING RECEIVED, THE "RX ON" LAMP INDICATES RECEIVED CARRIER ON, AND THE "RX DATA" LAMP INDICATES BINARY ONES IN THE RECEIVED MESSAGE.

*TO VIEW RECEIVED MESSAGE FRAMES USING THE BIT LEDS (RX SECTION)

1) SET RECEIVE MESSAGE THUMBWHEELS (RX SECTION) TO DESIRED FRAME WHERE POSITION "00" REPRESENTS THE PREFIX FRAME.

   THE BIT LED INDICATORS (RX SECTION) WILL SHOW THE CHARACTER BIT PATTERN FOR THE SELECTED FRAME

   SHOULD THERE BE A DIFFERENCE BETWEEN THE BITS IN THE TWO CHARACTERS COMPRISING THE SELECTED FRAME, THE APPLICABLE BIT LED(S) WILL BLINK.

   SINCE THE TWO CHARACTERS MAKING UP THE PREFIX FRAME ARE ZEROS AND ONES, RESPECTIVELY, ALL EIGHT, BIT LEDS WILL BLINK WHEN THE RECEIVE MESSAGE THUMBWHEELS (RX SECTION) ARE SET TO "00".

   NOTE THAT THE EIGHT, BIT LEDS (RX SECTION) ARE NOT EFFECTED BY THE POSITION OF THE AUX/HEX TOGGLE SWITCH (RX SECTION).

*TO VIEW RECEIVE MESSAGE FRAMES USING THE IN-LINE DISPLAY

1) SET AUX/HEX TOGGLE SWITCH (RX SECTION) TO HEX

2) SET RECEIVE MESSAGE THUMBWHEELS (RX SECTION) TO DESIRED FRAME

   THE FOUR DIGIT IN-LINE DISPLAY WILL ANNUNCIATE:

   DIGIT 1: FIRST FOUR BITS (HEXADECIMAL DECODING) IN THE FIRST CHARACTER IN THE SELECTED FRAME

   DIGIT 2: SECOND FOUR BITS (HEXADECIMAL DECODING) IN THE FIRST CHARACTER IN THE SELECTED FRAME

   DIGIT 3: FIRST FOUR BITS (HEXADECIMAL DECODING) IN THE FIRST CHARACTER IN THE SELECTED FRAME PLUS ONE

   DIGIT 4: SECOND FOUR BITS (HEXADECIMAL DECODING) IN THE FIRST CHARACTER IN THE SELECTED FRAME PLUS ONE

*TO VIEW THE NUMBER OF FRAMES RECEIVED

1) SET AUX/HEX TOGGLE SWITCH (RX SECTION) TO AUX

   THE IN-LINE DISPLAY WILL SHOW THE RECEIVED FRAME COUNT IN DIGITS 3 AND 4. THESE DIGITS WILL BE BLINKING.

Table 1. Test Set Operation

WILMINGTON COE

A. SET UP

1. CONNECTING TO UNIT-UNDER-TEST (UUT)

a. If test set is to be used to test 6800 logic (Central Station), connect test set to the communications terminals of the UUT with the INTERFACE cable that contains the integral 15-dB attenuation pad:

WIRE COLOR	TERMINAL
Red	TB2-3
Black	TB2-16
Green	TB2-2
White	TB2-15

b. If the test set is to be used to test 1802 logic (Remote Station), connect test set to connector J4 of UUT with the INTERFACE cable that does not contain the attenuation pad.

2. PROGRAMMING MODES

a. If the test set is to be used to test a Remote Station, DO NOT install plug connector P4B in PERSONALITY PROG receptacle connector J1.

b. If test set is to be used to test a Central Station, DO NOT remove plug connector P4B from PERSONALITY PROG receptacle connector J1.

Do not use plug for Remote Testing

c. Set AUTO/MANUAL switch to MANUAL.

B. USE AS CENTRAL STATION SIMULATOR

① AUX
② THUMB WHEELS T "00"
③ ENTER
④ TX

1. INITIALIZING TX FRAME COUNT

a. Set AUX/HEX switch to AUX.

b. Set FRAME SELECT switches to 01.

NOTE

Frame count and bit coding are defined in system manual (table A-1).

c. Press ENTER switch.

d. Observe that the left two digits of the hex display indicate number of frames to be transmitted.

FOR TESTING SLAVE STATION:

① USE CABLE WITHOUT ATTENUATOR

② INSTALL PERSONALITY PLUG Prog:

③ USE STATION ID 00000001 OFF SHORE or #1
00000010 P.D or #2
Preclose Dock

Start on Page 10
④ PROGRAM AS PER PAGE 10 & 11

⑤ AT STEP 4 PAGE 11 DISREGARD 4
TX DATA. INITIATE

Distat is central
Tide Gauges are Remotes
Slave central (Receives data & display it only)

TESTER S1

Table 1 Continued

OFF SHORE 11100001 00111011

P.D. 11100010 10111011

NOTE

Prefix frame 00 is transmitted automatically and, therefore, is not included in frame count.

2. LOADING TRANSMIT BUFFER

a. Set AUX/HEX switch to HEX.

b. Set FRAME SELECT switches to 01.

c. Set bit switches for "update and respond" of desired Remote Station address. For example, Remote Station No. 5 would be as follows:

```
0  0 0  0 0 1 0 1
|  |        |
|  |        +------------- Remote Station address
|  +---------------------- Reference freeze No.
+------------------------- Update and respond
```

1110001 for OFF SHORE
10 for P.D

d. Press ENTER switch.

e. Observe that transmit bit indicators 0-7 display the corret bit pattern.

3. TRANSMITTING INTERROGATION MESSAGE

a. Press TX INITIATE switch.

b. Observe that TX ON indicator lights and then goes out, indicating carrier presence.

c. Observe that TX DATA indicator blinks, indicating message content (1's and 0's).

4. CHECKING REMOTE STATION RESPONSE

a. Observe that the RX ON indicator lights and then goes out, indicating carrier presence.

b. Observe that the RX DATA indicator blinks, indicating message content.

c. Observe that the MSG VALID indicator lights (valid message received).

d. Set AUX/HEX switch to AUX and observe that the right two digits of the hex display indicate the number of frames received from the selected Remote Station (03).

Table 1 Continued

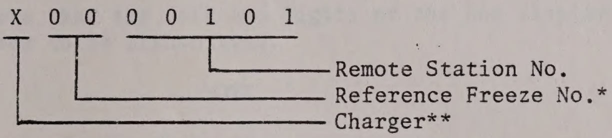
e. Set AUX/HEX switch to HEX and sequentially check received message frame contents by setting RECEIVE MSG switches as follows:

NOTE

The receive bit indicators will display the bit pattern of the selected frame. (A blinking indicator denotes that a different logic state exists for that bit between characters A and B of the selected frame. The hex display will indicate the value of the selected frame and the next successive frame.

00 - Prefix Frame (blinking)*
* Blinking because character A is all logic 0's and character B is all logic 1's; all other frames should have identical bits in characters A and B.

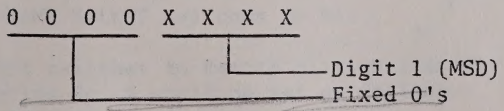
01 - Remote Station Identity Frame


X 0 0 0 0 1 0 1
Remote Station No.
Reference Freeze No.*
Charger**

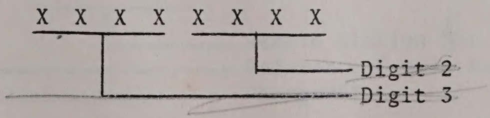
* Should be same as transmitted

** 1 = Alarm
0 = Normal

02 - Tide Level Data Frame


0 0 0 0 X X X X
Digit 1 (MSD)
Fixed 0's

03 - Tide Level Data Frame


X X X X X X X X
Digit 2
Digit 3

C. USE AS REMOTE STATION SIMULATOR

1. CLEARING TRANSMIT BUFFER

a. Set AUX/HEX switch to HEX.

b. Set FRAME SELECT switches to 00.

c. Press ENTER switch.

2. INITIALIZING TX FRAME COUNT

a. Set AUX/HEX switch to AUX.

b. Set FRAME SELECT switches to 03.

NOTE

Frame count and bit coding are defined in system manual (table A-1).

c. Press ENTER switch.

d. Observe that the left two digits of the hex display indicate number of data frames to be transmitted.

NOTE

Prefix frame 00 is transmitted automatically and, therefore, is not included in frame count.

3. LOADING TRANSMIT BUFFER

a. Set AUX/HEX switch to HEX.

b. Set FRAME SELECT switches to 01.

c. Set bit switches to Remote Station identity frame code. For example, Remote Station No. 5 would be set as follows:

```
X  0  0   0  0  1  0  1
|  |         |
|  |         └───────────── Remote Station No.
|  └─────────────────────── Reference Freeze No. *
└────────────────────────── Charger**
```

40.0
20.2
19.8

2
2
4

40.0
22.1
18.9

40.0
22.2
17.8

20.2
- 40
0

40.0
2 20.1
19.9

202

Table 1 Continued

* On power up, the Remote Station
Freeze Reference is initialized
to zero.

** 1 = Alarm
0 = Normal

d. Press ENTER switch.

e. Observe that transmit bit indicators display correct bit pattern.

f. Set FRAME SELECT switches to 02.

g. Set bit switches for some arbitrary tide level value, say 33.4 feet:

```
0  0  0  0   0  0  1  1
──────────   ──────────
     │           │
     │           └─────── Digit 1 (3)
     └─────────────────── Fixed Zeros
```

0000 0010

h. Press ENTER switch.

i. Observe that transmit bit indicators display correct bit pattern.

j. Set FRAME SELECT switches to 03.

k. Set bit switches for the balance of the tide level value:

```
0  0  1  1   0  1  0  0
──────────   ──────────
     │           │
     │           └─────── Digit 3 (4)
     └─────────────────── Digit 2 (3)
```

whatever I want
0010 0010

l. Press ENTER switch.

m. Observe that transmit bit indicators display correct bit pattern.

4. TRANSMITTING REMOTE DATA MESSAGE

In TL1S operation, the Remote Station (test set) may be interrogated automatically or by operator initiation. This example is an operator initialed request to a specific Remote Station.

Table 1 Continued

a. At Central Station control panel, press REQUEST switch.

b. Enter R05 on teleprinter keyboard. (Remote Station No. 5 as selected in paragraph C.3.c.)

c. Observe that the test set TX ON indicator lights and then goes out, indicating carrier presence.

d. Observe that TX DATA indicator blinks, indicating message contents.

e. Observe that 33.4 appears in the TIDE LEVEL display window at the Central Station control panel.

f. Observe that the KSR teleprinter printout shows 33.4 feet tide level for the selected station (test set).

Table A-2. Switch Setting/Jumper Data

A. SWITCH SETTING

PCB	SW	SECTION*							
		8	7	6	5	4	3	2	1
4120AA	S1	-	-	-	-	1	1	1	1
4120AA	S2	X	0	0	0	0	0	0	0
4124AA	S1	X	X	X	X	X	X	X	X
4110AC	S1	-	-	-	-	1	0	0	0

* LEGEND:
0 = SWITCH ON
1 = SWITCH OFF
X = IRRELEVANT

B. JUMPER DATA*

PCB	NOTE	JUMPER
4124AA	7	Y TO Z
4124AA	3	V TO W
4110AC	10	A TO C
4110AC	4	X TO Z

*REFER TO LOGIC DIAGRAM AND
PARTS LOCATION DRAWING

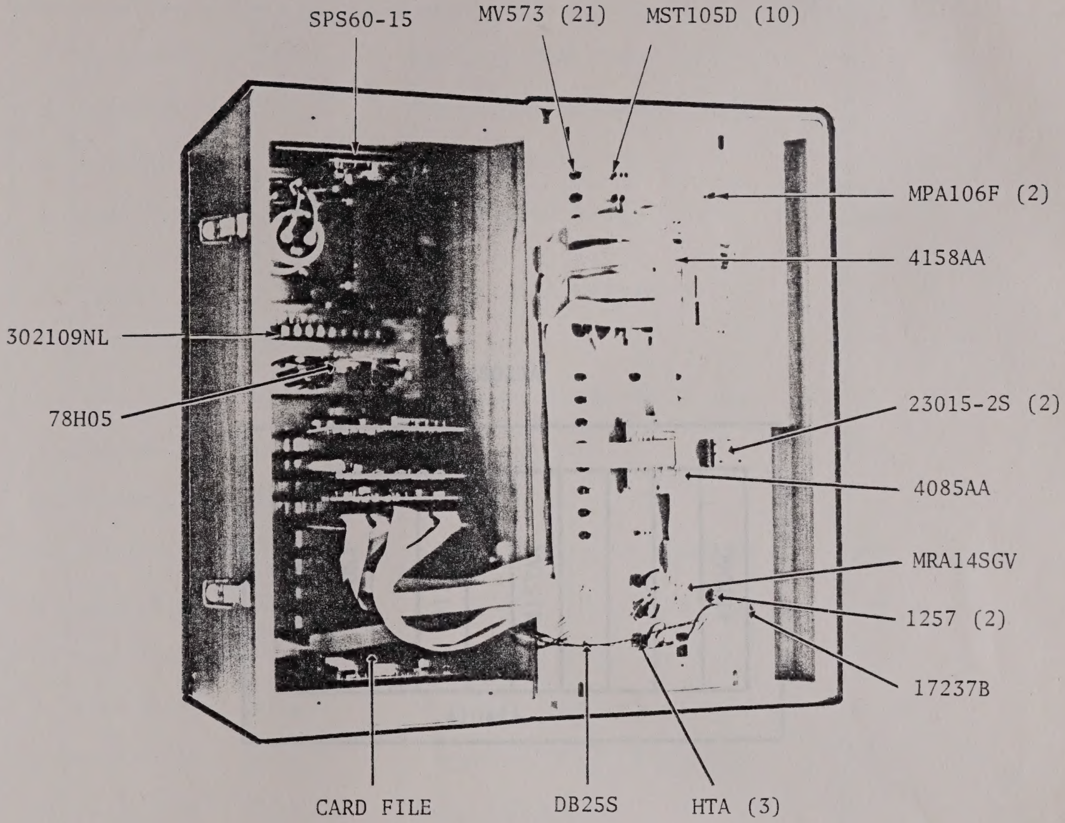

SPS60-15
MV573 (21)
MST105D (10)
MPA106F (2)
4158AA
302109NL
78H05
23015-2S (2)
4085AA
MRA14SGV
1257 (2)
17237B
CARD FILE
DB25S
HTA (3)

Figure 1. Test Set, Interior View

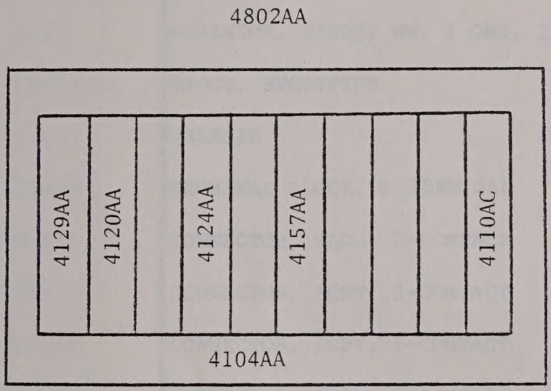

4802AA
4129AA
4120AA
4124AA
4157AA
4110AC
4104AA

Figure 2. Card File, PCB Locations

Table 3. Test Set Parts List

BILL OF MATERIAL				NAME CENTRAL/REMOTE TEST SET ASSY	NO. BM4802AA03
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4803AA00	ESI	ASSY, CONTROL PANEL, TEST SET	
2	1	4158AA00	ESI	PCB, PANEL INTERCONNECTION	
3	1	4157AA00	ESI	PCB, PANEL CONTROLLER	
4	1	SPS60-15	STANDARD POWER	ASSY, POWER SUPPLY	PS1
5	1	78H05	FAIRCHILD	IC, VOLTAGE REGULATOR	VR1
6	1	6169-B-2	THERMALOY	HEATSINK	
7	1	RH25	DALE	RESISTOR, FIXED, WW, 1 OHM, 25W	R1
8	1	1N1199A	MOTOROLA	DIODE, RECTIFIER	CR1
9	1	4951AC00	ESI	CHASSIS	
10	1	302109NL	MAGNUM	TERMINAL BLOCK, 9 TERMINAL	TB1
11	1	03-09-2021	MOLEX	CONNECTOR, PLUG, 2-CONTACT	J2
12	1	03-09-1021	MOLEX	CONNECTOR, RCPT, 2-CONTACT	P2
13	2	03-09-1052	MOLEX	CONNECTOR, RCPT, 5-CONTACT	P1,P3
14	1	03-09-2052	MOLEX	CONNECTOR, PLUG, 5-CONTACT	J1
15	2	03-09-2118	MOLEX	PINS, CONNECTOR	
16	7	02-09-1118	MOLEX	SOCKETS, CONNECTOR	
17	5	02-09-2133	MOLEX	PINS, CONNECTOR	
18	4	84-20-060-10	SOUTHCO	FASTENERS, FRACTIONAL TURN, NO. 84	
19	1	4104AA01	ESI	ASSY, MOTHER BOARD	
20	1	4124AA04	ESI	PCB, SYSTEM CONTROLLER	
21	1	4120AA02	ESI	PCB, SYSTEM MEMORY	
22	1	4110AC00	ESI	PCB, TEST SET MODEM	
23	1	4129AA01	ESI	PCB, POWER CONTROLLER	
24	2	FPB-163	ROBINSON NUGENT	COMPONENT CARRIER, 16-PIN	

Table 3 Continued

BILL OF MATERIAL	NAME CENTRAL/REMOTE TEST SET ASSY	NO. BM4802AA03

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
25	1	NPN	WOODCRAFT	CARRYING CASE, WOODEN	
26				DELETED	P4A
27	1	4805AD00	ESI	PERSONALITY PLUG, REMOTE	P4B
28	1	MRA14PGHVL	WINCHESTER	CONNECTOR, PLUG, 14-PIN	P5
29	2	AGC4	BUSS	FUSE, FAST-BLOW 5A, 12VDC	F1,2
30	1	MDL2	BUSS	FUSE, SLOW-BLOW, 2A, 117VAC	F3
31	2	2147	SMITH	GROMMET	
32	14	NPN	COML	MACHINE SCREW, FH, CRES NO. 8-32 x 3/4 IN.	
33	14	NPN	COML	WASHER, LOCK CRES NO. 8	
34	14	NPN	COML	WASHER, FLAT, CRES, NO. 8	
35	4	HW16	PREMIER	MACHINE SCREW, BINDER HEAD, NO. 10-32 x 1 IN. (WITH NYLON WASHER)	
36	2	4978AA00	ESI	BRACKET, MTG, PCB, CONNECTOR	
37	2	150D105X 9035A2	SPRAGUE	CAPACITOR, 1uF, 35V	C1,C2
38	1 PR	4953AA00	ESI	RAILS, MTG	
39	6	NPN	ESI	ASSY, RIBBON CABLE, 1 TO 1.5 FT LONG WITH DIP PLUGS	W1-W6

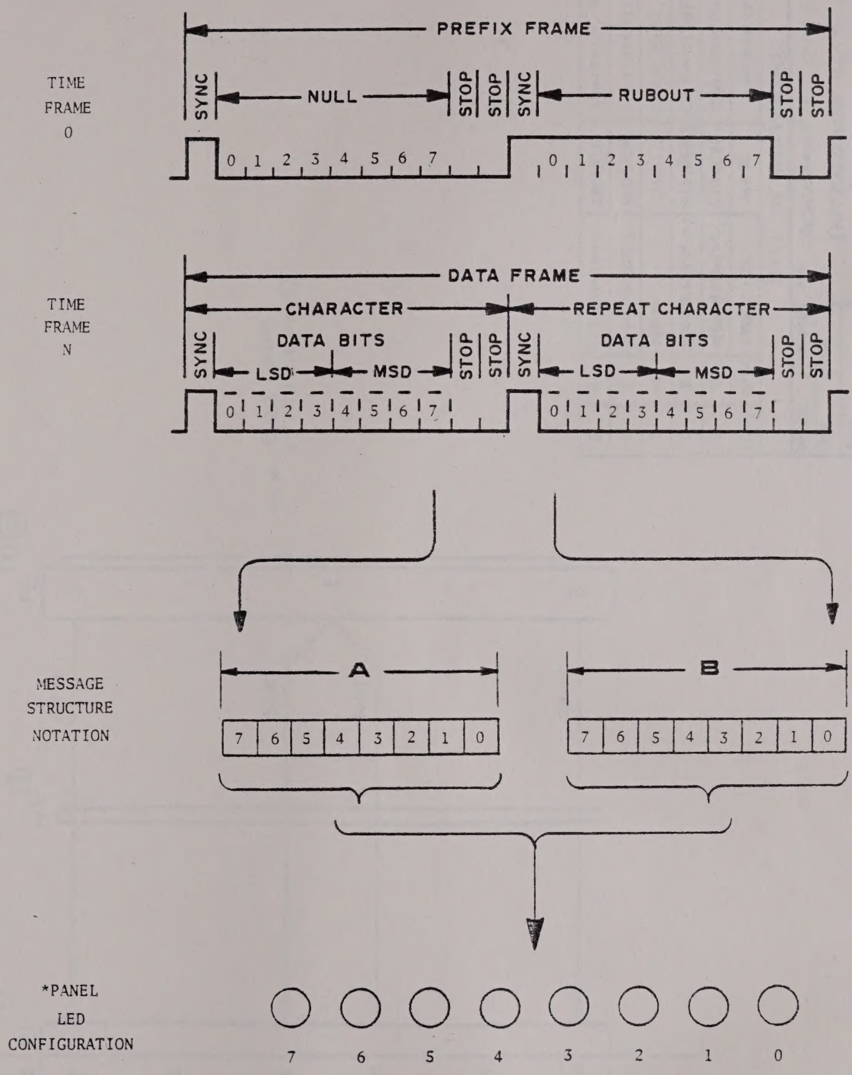
Table 4. Control Panel Parts List

BILL OF MATERIAL	NAME TEST SET CONTROL PANEL	NO. BM4803AA02

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4981AA00	ESI	FRONT PANEL, TEST SET	
2	1	6P-4	HEYCO	CLAMP, CABLE, STRAIN RELIEF	
3	1	17237B	BELDEN	ASSY, AC POWER CABLE	W10
4	3	HTA	BUSS	FUSEHOLDER	XF1 - XF3
5	1	1257RED	LEXAN	BINDING POST, 5-WAY	(+)
6	1	1257BLK	LEXAN	BINDING POST, 5-WAY	(-)
7	1	MRA14SGV	WINCHESTER	CONNECTOR, 14-PIN	J2
8	1	00-6022-044-450-001	ELCO	CONNECTOR, PC EDGE, 44-PIN	J3
9	1	4979AA00	ESI	BRACKET, MTG, CONNECTOR	
10	2	3416-0000	3M	CONNECTOR, PLUG, 16-PIN DIP	W7P1,W8P1
11	3'	3365-15	3M	CABLE, RIBBON, 16 CONDUCTOR	W7,W8
12	1	03-09-1052	MOLEX	CONNECTOR, RCPT, 5-CONTACT	W10P1
13	1	03-09-2052	MOLEX	CONNECTOR, PLUG, 5-CONTACT	J10
14	5	02-09-1118	MOLEX	SOCKETS, CONNECTOR	
15	5	02-09-2133	MOLEX	PINS, CONNECTOR	
16	2	23015-2S	DIGITRAN	SWITCH, THUMBWHEEL	S5, S6
17	10	MST105D	ALCO	SWITCH, MINIATURE TOGGLE, SPDT	S3,S4, S7-S14
18	2	MPA106F	ALCO	SWITCH, MOMENTARY, SPDT, PUSH	S1,S2
19	21	MV5753	MONSANTO	LED, RED	DS1-DS21
20	1	4085AA01	ESI	PCB, DIGITAL DISPLAY	
21	4	NPN	COML	SCREW, MACH, PHILLIPS HD, NO. 4-40 x ¼ IN.	
22	4	2372	SMITH	SPACER, THD, NO. 4-40x ½ IN.	
23	1	910-60	GRIFFITH	BEZEL, DIGITAL DISPLAY	

Table 4 Continued

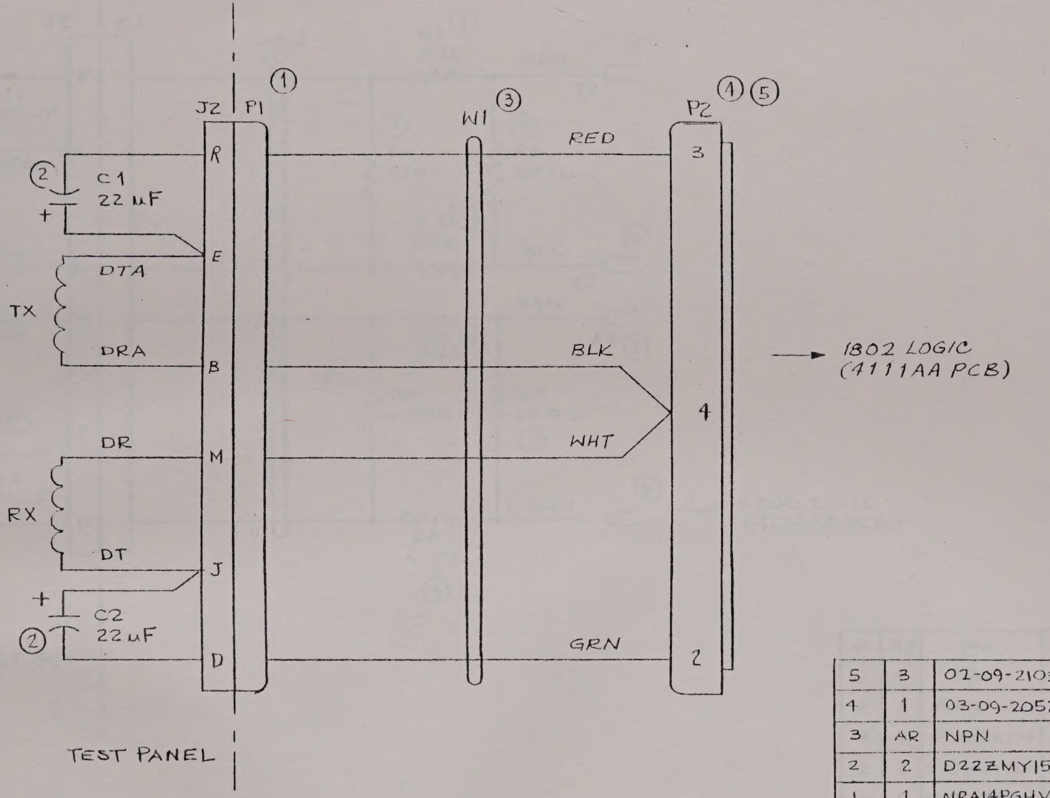
BILL OF MATERIAL				NAME TEST SET CONTROL PANEL	NO. BM4803AA02
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
24	1	DB25S	CANNON	SOCKET	J1
25	1	D20418-2	CANNON	MOUNTING KIT	
26	4	NPN	COML	WASHER, LOCK, NO. 4	


PREFIX FRAME
TIME FRAME 0
SYNC
NULL
STOP
STOP
SYNC
RUBOUT
STOP
STOP
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
DATA FRAME
TIME FRAME N
CHARACTER
REPEAT CHARACTER
SYNC
DATA BITS
LSD
MSD
STOP
STOP
SYNC
DATA BITS
LSD
MSD
STOP
STOP
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
MESSAGE STRUCTURE NOTATION
A
B
7 6 5 4 3 2 1 0
7 6 5 4 3 2 1 0
*PANEL LED CONFIGURATION
7 6 5 4 3 2 1 0

NOTES:

*LED WILL BLINK IF STATE OF BIT IN CHARACTER A DOES NOT AGREE WITH STATE OF CORRESPONDING BIT IN CHARACTER B.

Figure 3. Message, Frame, and Bit Definitions


J2
P1
①
W1
③
P2
④ ⑤
RED
BLK
WHT
GRN
R
E
B
M
J
D
3
4
2
② C1 22 uF
+
DTA
TX
DRA
DR
RX
DT
+
② C2 22 uF
TEST PANEL
1802 LOGIC
(4111AA PCB)

5	3	02-09-2103	MOLEX	CONTACT, PINS
4	1	03-09-2052	MOLEX	CONNECTOR, PLUG
3	AR	NPN	COML	WIRE, ELEC, INSUL, #22AWG
2	2	D222MY15M	SIEMENS	CAPACITOR, 22 uF, 15V
1	1	NRA14PGHVL,	WINCH.	CONNECTOR, PLUG
ITEM	QTY	PART NO.	MFR	DESCRIPTION

BILL OF MATERIAL

DR RC	DATE 1/19/9	TITLE SCHEMATIC DIAGRAM INTERFACE CABLE, TEST SET
APPR	DATE	
ISSUE 01		

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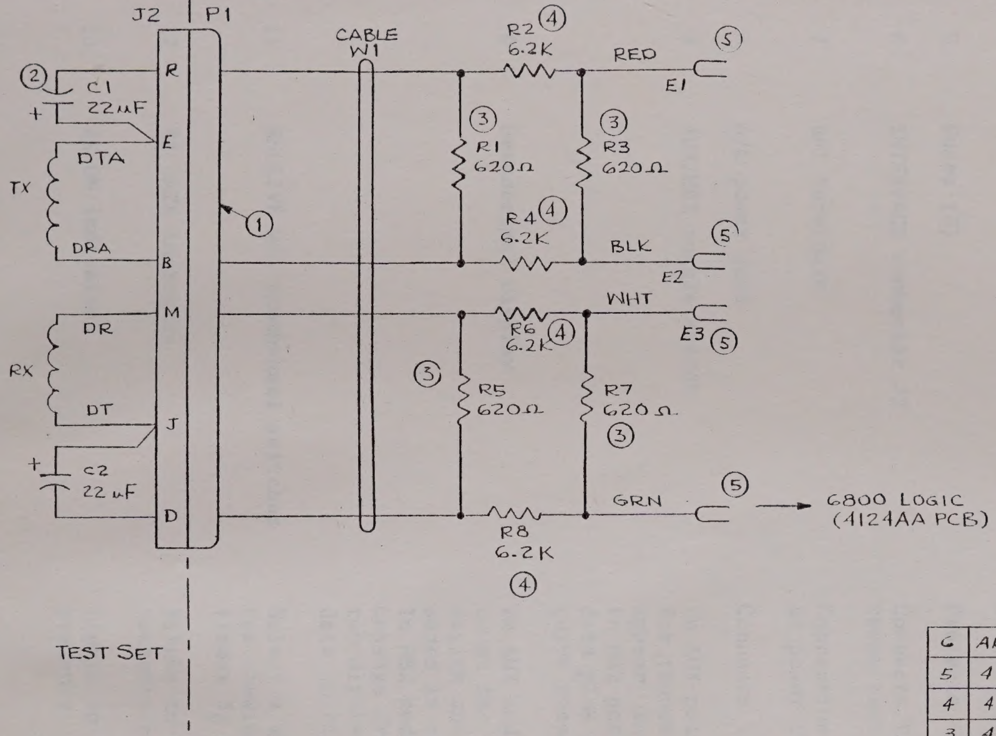
ENGINEERED SYSTEMS, INC.
PHOENIX, ARIZONA

DWG. NO. SD4807AA
SHEET

Figure 3A. Test Set INTERFACE Cable, Schematic Diagram


J2
P1
R
E
B
M
J
D
C1
22μF
C2
22μF
+
DTA
DRA
DR
DT
TX
RX
CABLE
W1
R1
620Ω
R2
6.2K
R3
620Ω
R4
6.2K
R5
620Ω
R6
6.2K
R7
620Ω
R8
6.2K
①
②
③
④
⑤
RED
BLK
WHT
GRN
E1
E2
E3
6800 LOGIC
(4124AA PCB)
TEST SET

6	AR	NPN	COML	WIRE, ELEC, INSUL #22 AWG
5	4	NPN	COML	SPADE LUG, NO. 6
4	4	RC07GF622J	COML	RESISTOR, 6.2K, 1/8W, 5%
3	4	RC05GF621J	COML	RESISTOR, 620Ω, 1/8W, 5%
2	2	D22ZMY15M	SIEMENS	CAPACITOR, 22μF, 15V
1	1	MRA14PGHVL	WINCH.	CONNECTOR, PLUG
ITEM	QTY	PART NO.	MFR	DESCRIPTION

BILL OF MATERIAL

DR RC	DATE 1/1[illegible]	TITLE SCHEMATIC DIAGRAM INTERFACE CABLE, 30 dB, TEST SET
APPR	DATE	
ISSUE 01		
ENGINEERED SYSTEMS, INC. PHOENIX, ARIZONA		DWG. NO. SD4806AA SHEET

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Figure 3B. Test Set 15-dB INTERFACE Cable, Schematic Diagram

Table 5. Operating Controls, Indicators, and Connectors

INDEX NO.	NAME	FUNCTION
1	Transmit bit indicators 0 thru 7	Indicate bit pattern of selected frame (index 16) in transmit buffer.
2	MSG VALID indicator	When lit indicates received message is valid.
3	Receive bit indicators 0 thru 7	Indicate bit pattern of selected frame (index 11) in receive buffer.
4	PERSONALITY PROG connector J1	Programs logic for Remote Station test or Central Station test by presence or absence of mating plug connector P4B.
5	Fuses (3)	Protects +5V, +12V, and ac line circuits.
6	INTERFACE connector J2	Connects TX and RX audio to cable between test set and unit-under-test (UUT).
7	BAT terminals	Connection points for 12 volts dc when ac power is not available.
8	A/C power cord	Connects 120-volt ac power to test set.
9	AUX/HEX toggle switch	In AUX position, enables frame count for transmit and receive messages to appear in hex display (index 10). In HEX position, enables selected frame data plus succeeding frame data of receive message to appear in hex display.
10	Hexadecimal display	In AUX mode (index 9), displays frame count for transmit message in left two digits and frame count for receive messages in right two digits. In HEX mode, displays selected receive message frame data (index 11) in left two digits and selected frame-plus-one data in right two digits.
11	RECEIVE MSG thumbwheel switches	Select a specific receive message frame for viewing on receive bit indicators (index 3) and hex display (index 10).
12	RX DATA indicator	Blinks to indicate the logic 1 and 0 contents of message being received.
13	RX ON indicator	Lights to indicate receive carrier presence.

Table 5 Continued

INDEX NO.	NAME	FUNCTION
14	AUTO/MANUAL toggle switch	In MANUAL position, permits operator to transmit a single message with TX INITIATE switch (index 15). In AUTO position, enables test set logic to repeatedly transmit the message in the transmit buffer at 5-second intervals.
15	TX INITIATE momentary switch	When pressed causes message in transmit buffer to be sent to UUT.
16	FRAME SELECT thumbwheel switches	In AUX mode (index 9), permit operator to condition transmit buffer logic to accept exact quantity of frames to be transmitted. In HEX mode, permit operator to select frame number for bit pattern established by setting bit switches (index 20).
17	ENTER momentary switch	When pressed causes bit pattern of bit switches (index 20) to be placed in transmit buffer at the storage location determined by the setting of FRAME SELECT switches (index 16).
18	TX ON indicator	Lights to indicate transmit carrier presence.
19	TX DATA indicator	Blinks to indicate the logic 1 and 0 content of message being received.
20	Bit toggle switches 0 thru 7	Permit operator to construct bit pattern of transmit frame determined by setting of FRAME SELECT switches (index 16).

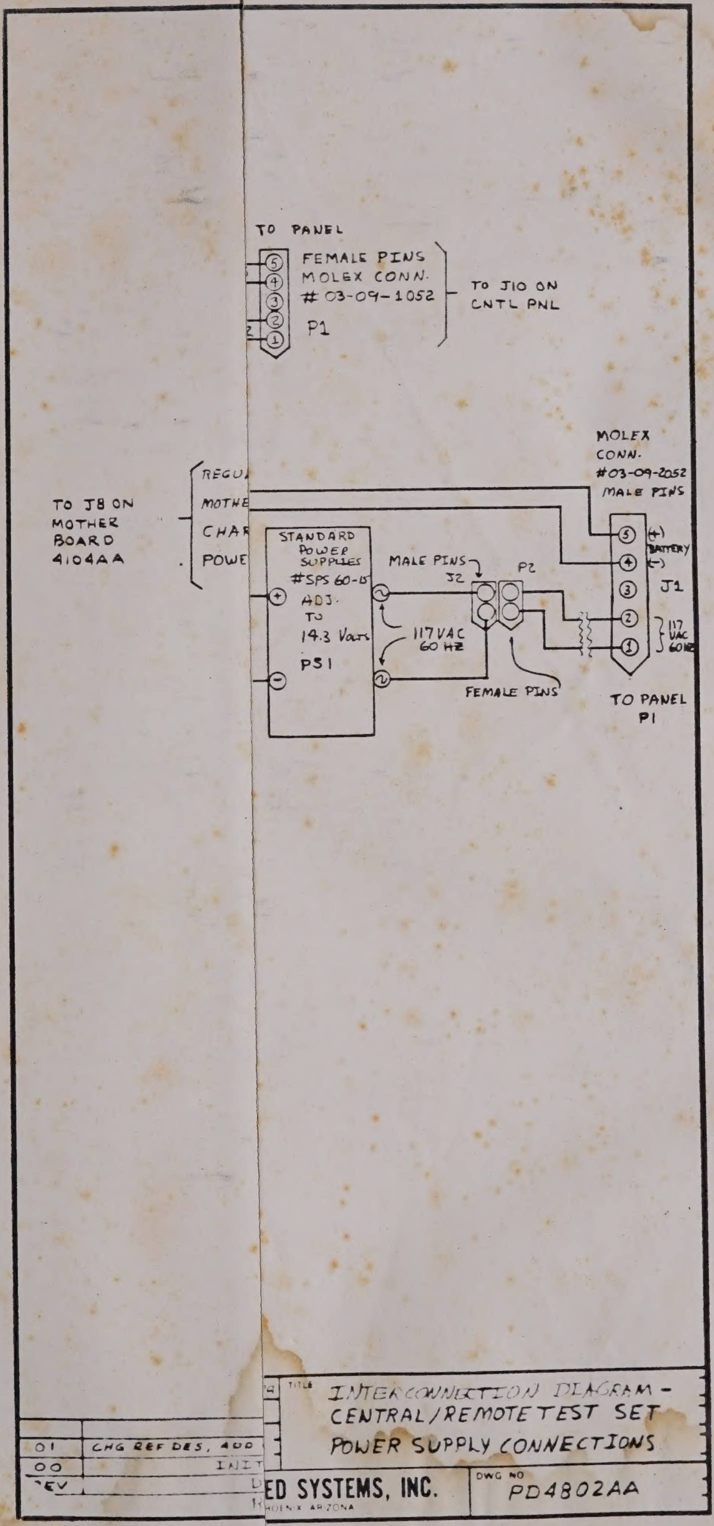
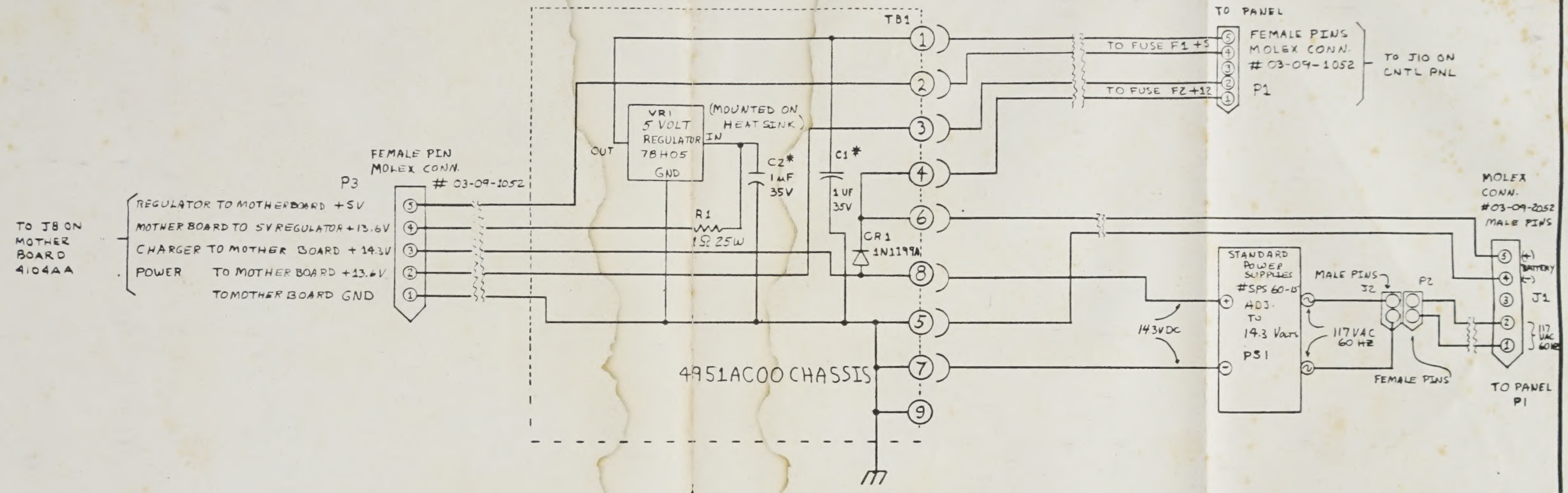

TO PANEL
FEMALE PINS
MOLEX CONN.
# 03-09-1052
P1
TO J10 ON
CNTL PNL
MOLEX
CONN.
#03-09-2052
MALE PINS
TO J8 ON
MOTHER
BOARD
4104AA
REGU
MOTHE
CHAR
POWE
STANDARD
POWER
SUPPLIES
#SPS 60-15
ADJ.
TO
14.3 Vdc
PS1
MALE PINS
J2
P2
117VAC
60 HZ
FEMALE PINS
(+)
BATTERY
(−)
J1
117
VAC
60HZ
TO PANEL
P1
01
CHG REF DES, ADD
00
INIT
REV
TITLE
INTERCONNECTION DIAGRAM -
CENTRAL/REMOTE TEST SET
POWER SUPPLY CONNECTIONS
ED SYSTEMS, INC.
PHOENIX ARIZONA
DWG NO
PD4802AA

Figure 7. Power Distribution, Interconnection Diagram


TO J8 ON MOTHER BOARD 4104AA
REGULATOR TO MOTHERBOARD +5V
MOTHER BOARD TO 5V REGULATOR +13.6V
CHARGER TO MOTHER BOARD +14.3V
POWER TO MOTHER BOARD +13.6V
TO MOTHER BOARD GND
FEMALE PIN MOLEX CONN.
P3
# 03-09-1052
5
4
3
2
1
VR1
5 VOLT REGULATOR
78H05
GND
IN
OUT
(MOUNTED ON HEAT SINK)
C2*
1uF
35V
C1*
1 UF
35V
R1
1Ω 25W
CR1
1N1199A
TB1
1
2
3
4
6
8
5
7
9
4951AC00 CHASSIS
TO PANEL
TO FUSE F1 +5
TO FUSE F2 +12
FEMALE PINS
MOLEX CONN.
# 03-09-1052
P1
TO J10 ON CNTL PNL
STANDARD POWER SUPPLIES
#SPS 60-15
ADJ. TO 14.3 Vdc
PS1
14.3VDC
117VAC 60 HZ
MALE PINS
J2
P2
FEMALE PINS
MOLEX CONN.
#03-09-2052
MALE PINS
(+)
BATTERY
(-)
J1
117 VAC 60HZ
TO PANEL
P1

* C1, C2 INSTALLED ON REGULATOR HEATSINK

01	CHG REF DES, ADD C2, ADD NOTE (A064)	RC	10/19/8
00	INITIAL RELEASE	DLF	5/25/78
REV	DESCRIPTION	BY	DATE

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DR DLF 5-25-78

ISSUE 01

TITLE INTERCONNECTION DIAGRAM - CENTRAL/REMOTE TEST SET POWER SUPPLY CONNECTIONS

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA

DWG NO PD4802AA

Figure 7. Power Distribution, Interconnection Diagram

Figure 4. Control Panel, Controls

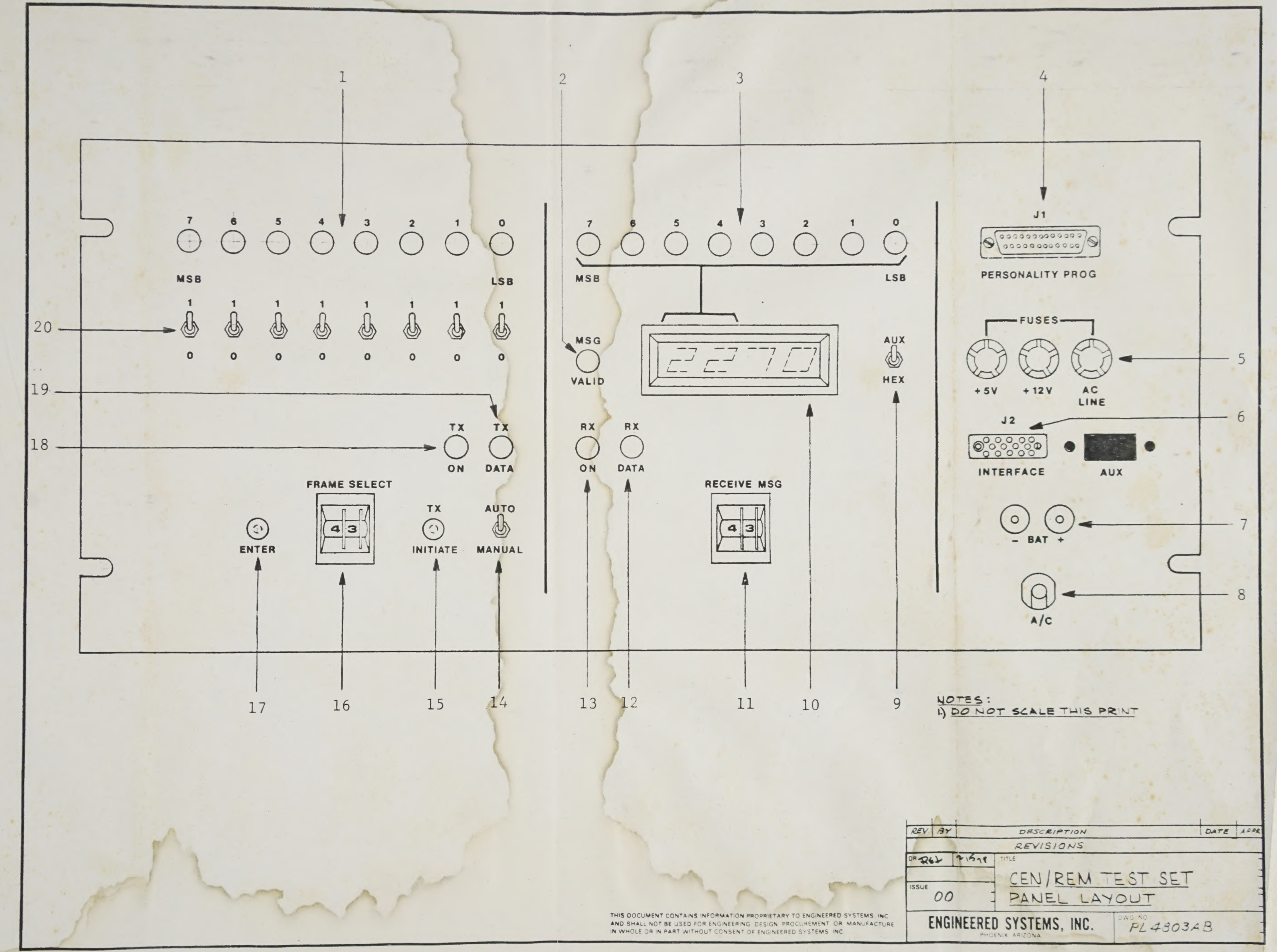
1
2
3
4
7 6 5 4 3 2 1 0
MSB
LSB
1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0
20
19
18
TX ON
TX DATA
FRAME SELECT
4 3
ENTER
TX INITIATE
AUTO MANUAL
MSG VALID
RX ON
RX DATA
7 6 5 4 3 2 1 0
MSB
LSB
2270
AUX HEX
RECEIVE MSG
4 3
J1
PERSONALITY PROG
FUSES
+5V
+12V
AC LINE
5
J2
6
INTERFACE
AUX
- BAT +
7
A/C
8
17
16
15
14
13
12
11
10
9
NOTES:
1) DO NOT SCALE THIS PRINT
REV
BY
DESCRIPTION
DATE
APPR
REVISIONS
DR
TITLE
CEN/REM TEST SET
PANEL LAYOUT
ISSUE
00
ENGINEERED SYSTEMS, INC.
PHOENIX, ARIZONA
DWG NO
PL4803AB
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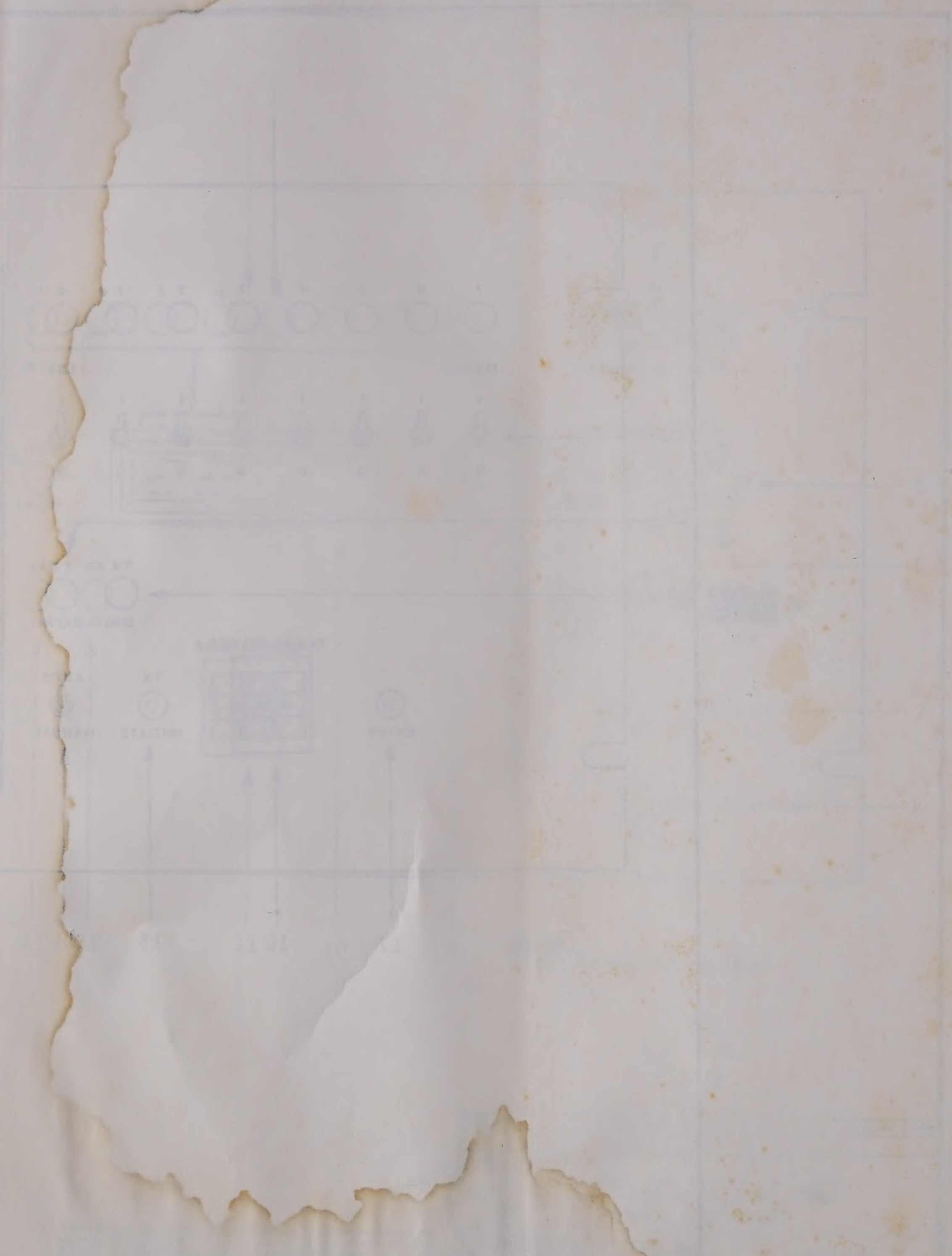
Figure 4. Control Panel, Controls and Indicators


XT
STATION

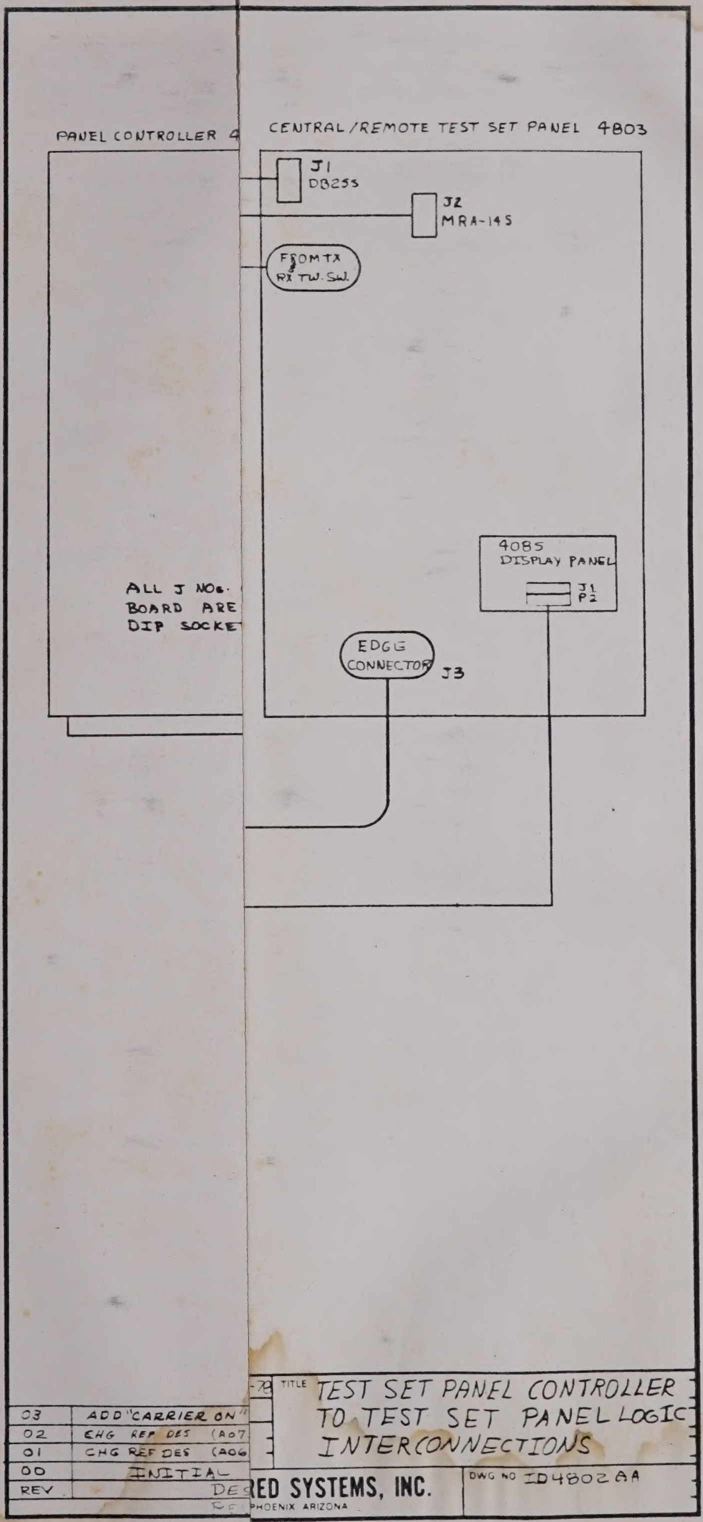

PANEL CONTROLLER 4
CENTRAL/REMOTE TEST SET PANEL 4803
J1
DB25S
J2
MRA-14S
FROM TX
RX TW. SW.
4085
DISPLAY PANEL
J1
P2
ALL J NOs.
BOARD ARE
DIP SOCKET
EDGE
CONNECTOR
J3
03
ADD "CARRIER ON"
02
CHG REF DES (A07
01
CHG REF DES (A06
00
INITIAL
REV
DES
-79
TITLE
TEST SET PANEL CONTROLLER
TO TEST SET PANEL LOGIC
INTERCONNECTIONS
RED SYSTEMS, INC.
PHOENIX ARIZONA
DWG NO
ID4802AA

Figure 5. Panel Controller/Control Panel, Interconnections

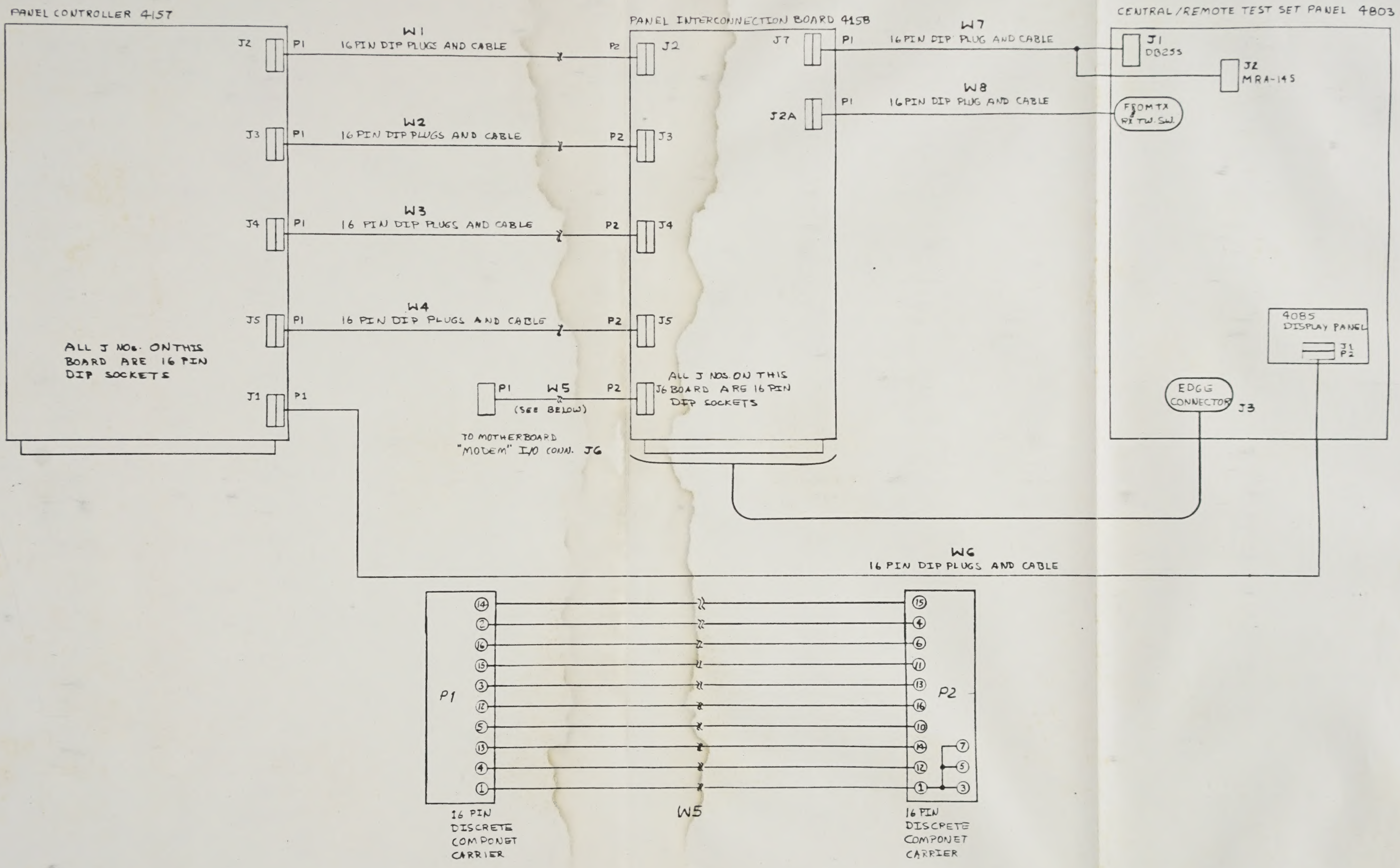

PANEL CONTROLLER 4157
J2
P1
W1
16 PIN DIP PLUGS AND CABLE
P2
J2
J3
P1
W2
16 PIN DIP PLUGS AND CABLE
P2
J3
J4
P1
W3
16 PIN DIP PLUGS AND CABLE
P2
J4
J5
P1
W4
16 PIN DIP PLUGS AND CABLE
P2
J5
ALL J NO. ON THIS BOARD ARE 16 PIN DIP SOCKETS
J1
P1
P1
W5
P2
(SEE BELOW)
J6
TO MOTHERBOARD "MODEM" I/O CONN. J6
PANEL INTERCONNECTION BOARD 4158
ALL J NOS. ON THIS BOARD ARE 16 PIN DIP SOCKETS
J7
P1
W7
16 PIN DIP PLUG AND CABLE
J2A
P1
W8
16 PIN DIP PLUG AND CABLE
CENTRAL/REMOTE TEST SET PANEL 4803
J1
DB25S
J2
MRA-14S
FROM TX RX TW. SW.
4085 DISPLAY PANEL
J1
P2
EDGE CONNECTOR
J3
W6
16 PIN DIP PLUGS AND CABLE
P1
⑭
②
⑯
⑮
③
⑫
⑤
⑬
④
①
W5
P2
⑮
④
⑥
⑪
⑬
⑯
⑩
⑭
⑫
①
⑦
⑤
③
16 PIN DISCRETE COMPONET CARRIER
16 PIN DISCRETE COMPONET CARRIER

Figure 5. Panel Controller/Control Panel, Interconnections

REV	DESCRIPTION	BY	DATE
03	ADD "CARRIER ON" LEAD (A094)	RC	12/20/8
02	CHG REF DES (A075)	GJF	10/30/8
01	CHG REF DES (A062)	RC	10/19/8
00	INITIAL RELEASE	DLF	5-30-78

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ISSUE

TITLE TEST SET PANEL CONTROLLER TO TEST SET PANEL LOGIC INTERCONNECTIONS

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA

DWG NO ID4802AA

① THUMB WHEELS TO "08"
② XMIT ENTER
③ "AUX"
④ XMIT FRAME "01"
⑤ ENTER
⑥ READ DISPLAY 01FF FLASHING
⑦ HEX
⑧ BIT SWITCHES 11100010 for Preachers Doen
11100001 for Off Shore

2.3.2 MASTER TO REMOTE MESSAGE DETAIL

INTERROGATION (2 FRAMES): PREFIX—ADDRESS

2.3.2.1 ADDRESS FRAME DEFINITION (FRAME 1)
(PREFIX FRAME IS FRAME 0)

BITS 7. RESPONCE MODE
0: UPDATE AND RESPOND (REMOTE STATION ADDRESS MUST BE CORRECT)
1: UPDATE ONLY (SYSTEM ADDRESS MUST BE CORRECT)

BITS 6-5: REFERENCE FREEZE NUMBER

BITS 4-3-2-1-0: ADDRESS FIELD
(SYSTEM ADDRESS = 1E (HEX)

10

2.3.3 REMOTE TO MASTER MESSAGE DETAIL

DATA RESPONSE: PREFIX---IDENTITY---DATA

① THUMB WHEELS TO 0
② XMIT ENTER
③ AUX
④ XMIT FRAME 01
⑤ ENTER
⑥ RCVD-DISPLAY DIFF
⑦ HEX
⑧ BITS ON SWITCHES

2.3.3.1 IDENTITY FRAME DEFINITION (FRAME 1)
(PREFIX FRAME IS FRAME 0)

BIT 7: CHARGER ALARM

BITS 6-5: REFERENCE FREEZE NUMBCR

BITS 4-3-2-1-0: IDENTITY FIELD

2.3.3.2 DATA FRAME DEFINITION

FRAME 2

BITS 7-6-5-4: FIXED ZEROS

BITS 3-2-1-0: DIGIT 1 (MOST SIGNIFICANT)

FRAME 3

BITS 7-6-5-4: DIGIT 2

BITS 3-2-1-0: DIGIT 3

2.3.2 MASTER TO REMOTE MESSAGE DETAIL

INTERROGATION (2 FRAMES): PREFIX—ADDRESS

2.3.2.1 ADDRESS FRAME DEFINITION (FRAME 1)
(PREFIX FRAME IS FRAME 0)

BITS 7: RESPONCE MODE
0: UPDATE AND RESPOND (REMOTE STATION ADDRESS MUST BE CORRECT)
1: UPDATE ONLY (SYSTEM ADDRESS MUST BE CORRECT)

BITS 6-5: REFERENCE FREEZE NUMBER

BITS 4-3-2-1-0: ADDRESS FIELD
(SYSTEM ADDRESS = 1E (HEX)

10

2.3.3 REMOTE TO MASTER MESSAGE DETAIL

DATA RESPONSE: PREFIX—IDENTITY—DATA

2.3.3.1 IDENTITY FRAME DEFINITION (FRAME 1)
(PREFIX FRAME IS FRAME 0)

BIT 7: CHARGER ALARM

BITS 6-5: REFERENCE FREEZE NUMBER

BITS 4-3-2-1-0: IDENTITY FIELD

① THUMB WHEELS TO 0
② XMIT ENTER
③ AUX
④ XMIT FRAME 01
⑤ ENTER
⑥ READ-DISPLAY 01FF
⑦ HEX
⑧ BITS @ SWITCHES

2.3.3.2 DATA FRAME DEFINITION

FRAME 2

BITS 7-6-5-4: FIXED ZEROS

BITS 3-2-1-0: DIGIT 1 (MOST SIGNIFICANT)

LEAVE PLUG OUT

FRAME 3

BITS 7-6-5-4: DIGIT 2

BITS 3-2-1-0: DIGIT 3

2.3.2 MASTER TO REMOTE MESSAGE DETAIL

INTERROGATION (2 FRAMES): PREFIX—ADDRESS

2.3.2.1 ADDRESS FRAME DEFINITION (FRAME 1)
(PREFIX FRAME IS FRAME 0)

BITS 7: RESPONCE MODE
0: UPDATE AND RESPOND (REMOTE STATION ADDRESS MUST BE CORRECT)
1: UPDATE ONLY (SYSTEM ADDRESS MUST BE CORRECT)

BITS 6-5: REFERENCE FREEZE NUMBER

BITS 4-3-2-1-0: ADDRESS FIELD
(SYSTEM ADDRESS = 1E (HEX)

10

2.3.3 REMOTE TO MASTER MESSAGE DETAIL

DATA RESPONSE: PREFIX—IDENTITY—DATA

2.3.3.1 IDENTITY FRAME DEFINITION (FRAME 1)
(PREFIX FRAME IS FRAME 0)

BIT 7: CHARGER ALARM

BITS 6-5: REFERENCE FREEZE NUMBER

BITS 4-3-2-1-0: IDENTITY FIELD

2.3.3.2 DATA FRAME DEFINITION

① THUMB WHEELS TO 0
② XMIT ENTER
③ AUX
④ XMIT FRAMES 01
⑤ ENTER
⑥ RCVD - DISPLAY 01FF
⑦ HEX
⑧ BITS @ SWITCHES

FRAME 2

BITS 7-6-5-4: FIXED ZEROS

BITS 3-2-1-0: DIGIT 1 (MOST SIGNIFICANT)

FRAME 3

BITS 7-6-5-4: DIGIT 2

BITS 3-2-1-0: DIGIT 3

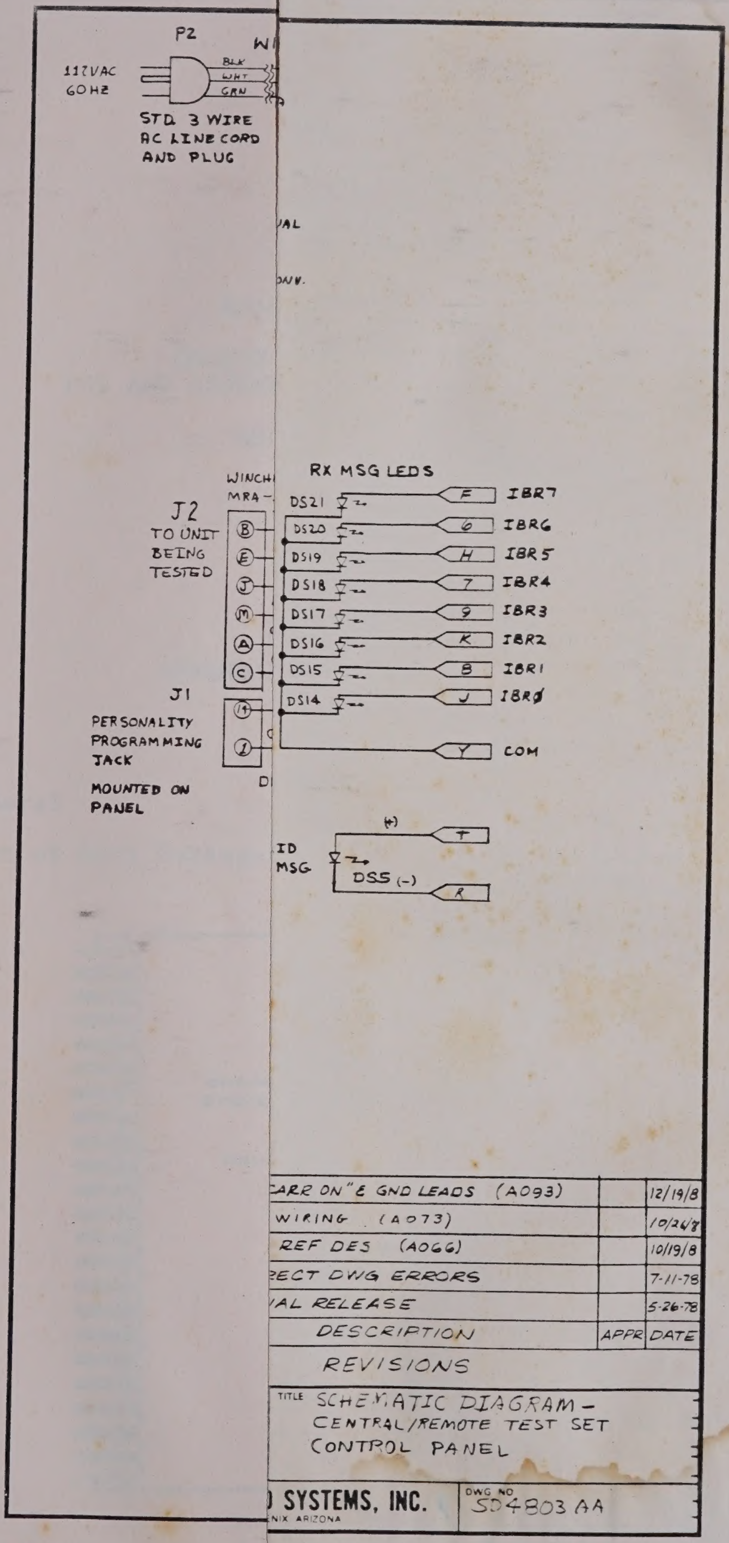
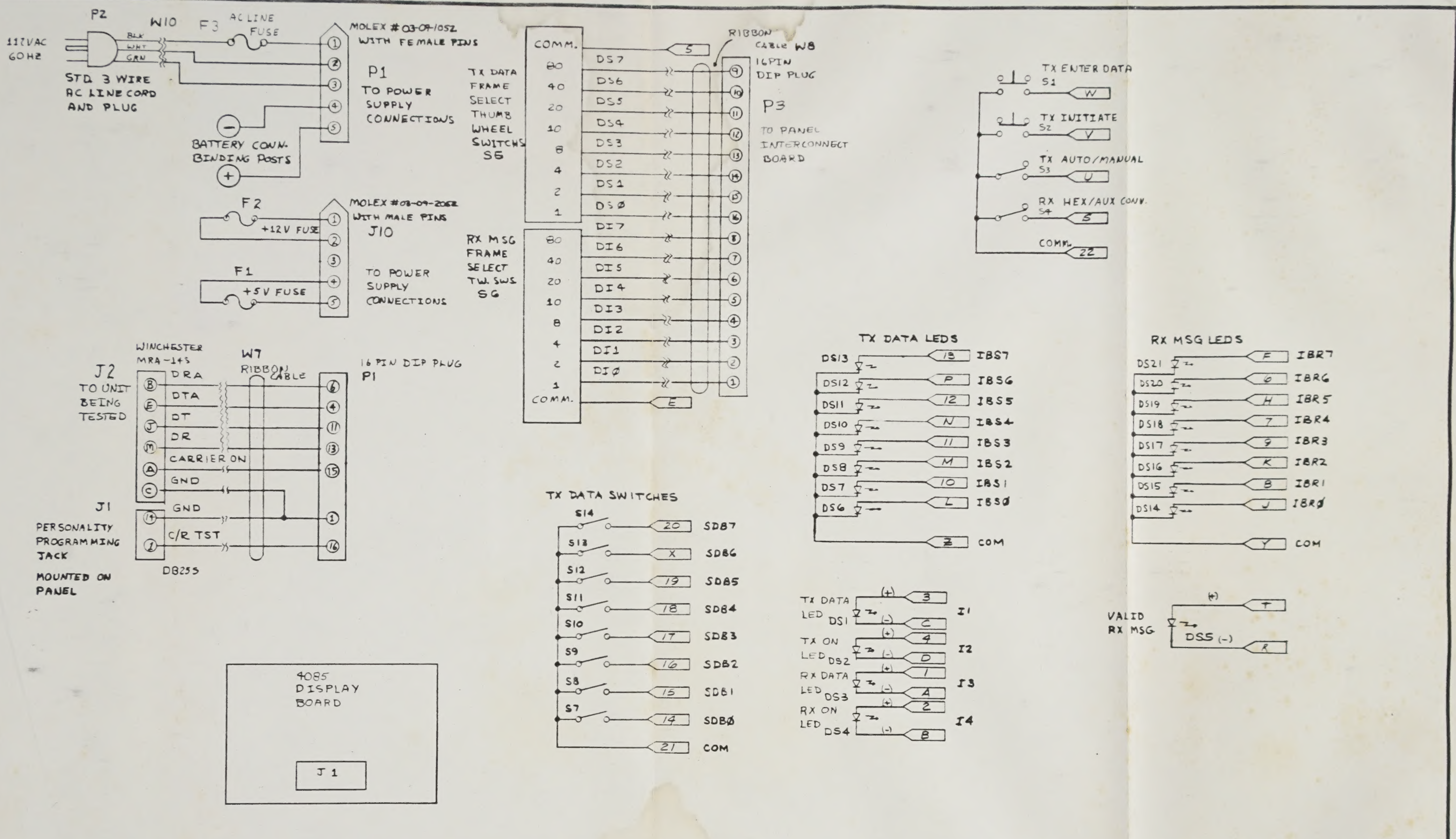

P2
112VAC
60 HZ
BLK
WHT
GRN
STD 3 WIRE
AC LINE CORD
AND PLUG
RX MSG LEDS
J2
TO UNIT
BEING
TESTED
B
E
J
M
A
C
J1
PERSONALITY
PROGRAMMING
JACK
MOUNTED ON
PANEL
DS21
DS20
DS19
DS18
DS17
DS16
DS15
DS14
F
6
H
7
9
K
B
J
Y
IBR7
IBR6
IBR5
IBR4
IBR3
IBR2
IBR1
IBRØ
COM
ID
MSG
DS5
(+)
(-)
T
R
ARR ON "E GND LEADS (A093) 12/19/8
WIRING (A073) 10/26/8
REF DES (A066) 10/19/8
ECT DWG ERRORS 7-11-78
AL RELEASE 5-26-78
DESCRIPTION
APPR
DATE
REVISIONS
TITLE SCHEMATIC DIAGRAM - CENTRAL/REMOTE TEST SET CONTROL PANEL
SYSTEMS, INC.
NIX ARIZONA
DWG NO
SD4803 AA

Figure 6. Control Panel, Schematic Diagram


117VAC 60HZ
P2
W10
F3
AC LINE FUSE
BLK
WHT
GRN
STD. 3 WIRE AC LINE CORD AND PLUG
MOLEX #03-09-1052 WITH FEMALE PINS
P1
TO POWER SUPPLY CONNECTIONS
BATTERY CONN. BINDING POSTS
F2
+12V FUSE
MOLEX #03-09-2062 WITH MALE PINS
J10
F1
+5V FUSE
TO POWER SUPPLY CONNECTIONS
TX DATA FRAME SELECT THUMB WHEEL SWITCHES S5
RX MSG FRAME SELECT T.W. SWS S6
COMM.
80
40
20
10
8
4
2
1
DS7
DS6
DS5
DS4
DS3
DS2
DS1
DSØ
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DIØ
RIBBON CABLE W8
16PIN DIP PLUG
P3
TO PANEL INTERCONNECT BOARD
TX ENTER DATA S1
TX INITIATE S2
TX AUTO/MANUAL S3
RX HEX/AUX CONV. S4
COMM.
WINCHESTER MRA-14S
J2
TO UNIT BEING TESTED
DRA
DTA
DT
DR
CARRIER ON
GND
J1
PERSONALITY PROGRAMMING JACK
MOUNTED ON PANEL
C/R TST
DB25S
W7
RIBBON CABLE
16 PIN DIP PLUG
P1
TX DATA LEDS
DS13
DS12
DS11
DS10
DS9
DS8
DS7
DS6
IBS7
IBS6
IBS5
IBS4
IBS3
IBS2
IBS1
IBSØ
COM
RX MSG LEDS
DS21
DS20
DS19
DS18
DS17
DS16
DS15
DS14
IBR7
IBR6
IBR5
IBR4
IBR3
IBR2
IBR1
IBRØ
COM
TX DATA SWITCHES
S14
S13
S12
S11
S10
S9
S8
S7
SDB7
SDB6
SDB5
SDB4
SDB3
SDB2
SDB1
SDBØ
COM
TX DATA LED DS1
TX ON LED DS2
RX DATA LED DS3
RX ON LED DS4
I1
I2
I3
I4
VALID RX MSG
DS5
4085 DISPLAY BOARD
J 1

NOTES:
1. SYMBOL ⊂ IS A PIN ON A PC BOARD CONN.

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REV	BY	DESCRIPTION	APPR	DATE
04	RC	ADD "CARR ON" & GND LEADS (A093)		12/19/8
03	GJF	CHG WIRING (A073)		10/26/8
02	RC	CHG REF DES (A066)		10/19/8
01	J.N.	CORRECT DWG ERRORS		7-11-78
00	DLF	INITIAL RELEASE		5-26-78

REVISIONS

DR DLF 5-26-78
TITLE SCHEMATIC DIAGRAM –
CENTRAL/REMOTE TEST SET
CONTROL PANEL
ISSUE 04

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA
DWG NO SD4803 AA

Figure 6. Control Panel, Schematic Diagram

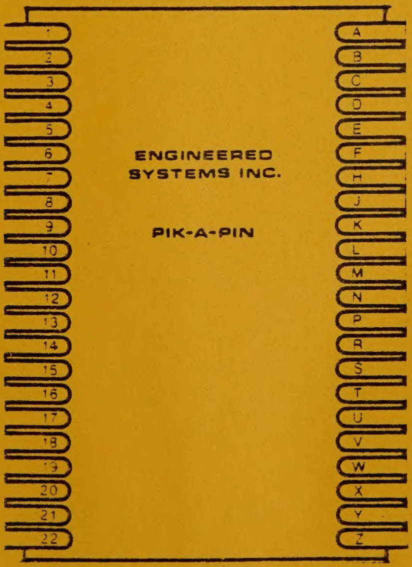
Appendix A

CM4000 TEST SET PCB AND ASSEMBLY DATA PACKAGES

AS4802AA

APPENDIX CONTENTS

Para		Page
A-1	General	A-2
A-2	List of Data Packages	A-2


ENGINEERED SYSTEMS INC.
PIK-A-PIN
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
W
X
Y
Z

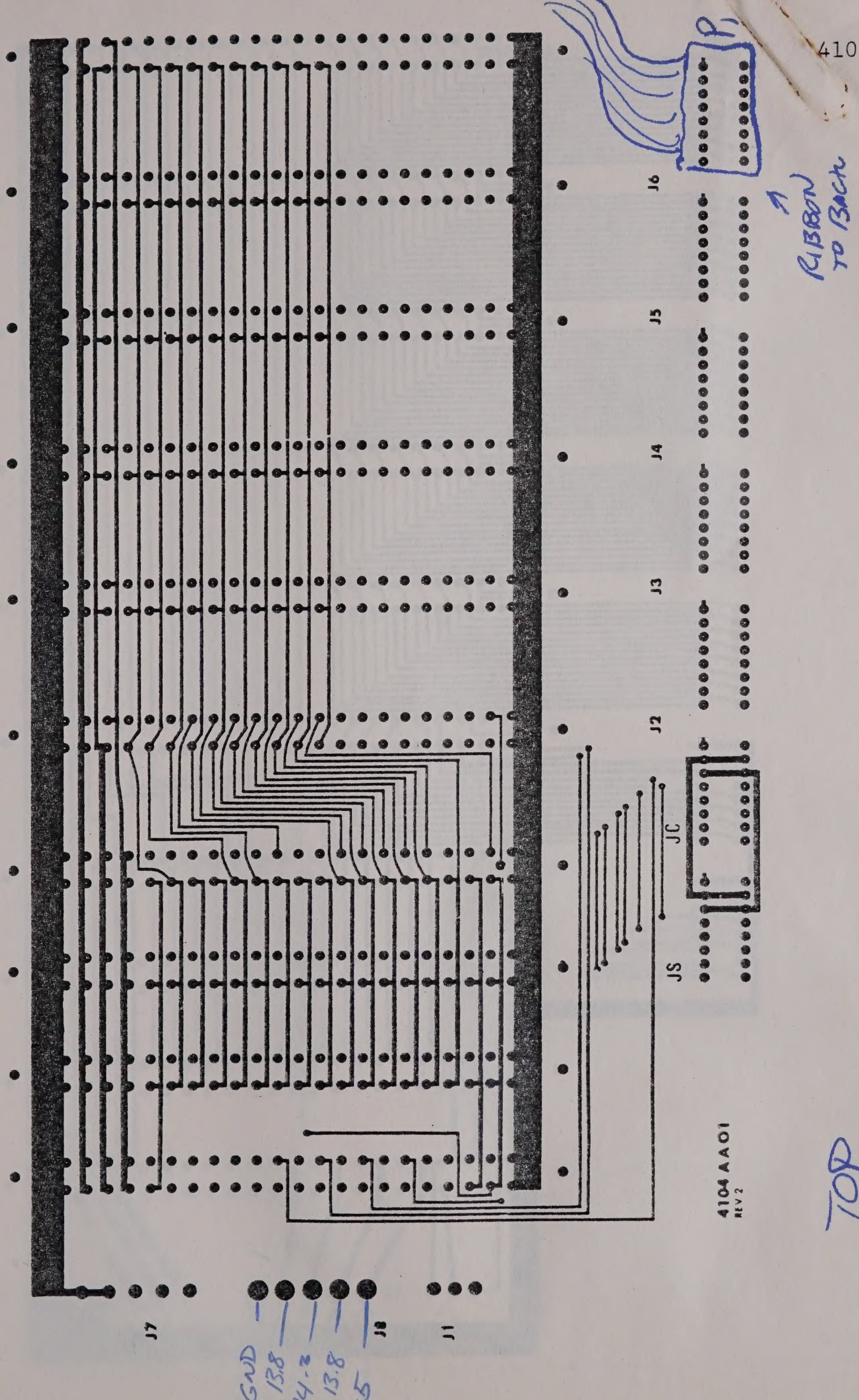
A-1. GENERAL

A-2. This appendix contains a PCB data package for each printed circuit board and major assembly used in the Test Set. Each data package includes a functional description, physical description, theory of operation, block diagram, logic diagram, bill of material and parts location drawing. Timing diagrams are used to supplement the theory of operation text when necessary.

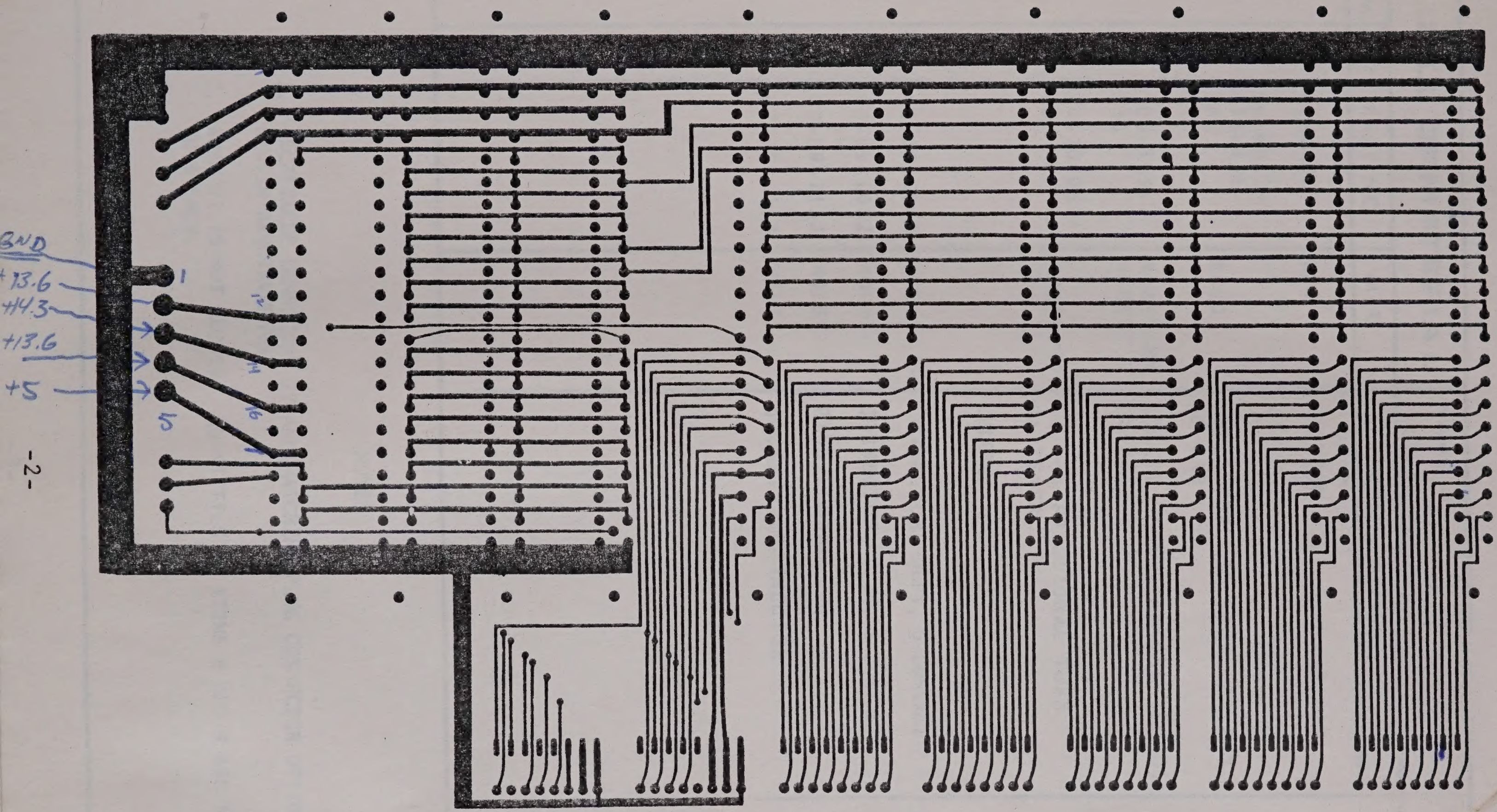
A-3. LIST OF DATA PACKAGES

A-4. The data packages are arranged in numerical sequence by part numbers in accordance with the following list:

Part No.	Name
4085AA	Digital Display PCB
4104AA	Mother Board Assy
4110AC	Test Set Modem PCB
4120AA	System Memory PCB
4124AA	System Controller PCB
4129AA	Power Controller PCB
4157AA	Panel Controller PCB
4158AA	Panel Interconnection PCB
4805AD	Remote Personality Plug Assy
SPS60-15	Power Supply Assy


P1
RIBBON TO BACK
J6
J5
J4
J3
J2
JC
JS
J7
J8
J1
GND
13.8
14.8
13.8
+5
4104AAO1
REV 2
TOP

Mother Board, Card File Side


GND
+13.6
+14.3
+13.6
+5
1
12
14
16
5

Mother Board, Wiring Side

BILL OF MATERIAL				NAME MOTHER BOARD	NO. BM4104AA04
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4104AA01	ESI	PRINTED WIRING BOARD G10	
2	10	00-6022-044-451-001	ELCO	CONNECTOR, PC EDGE, 44 PIN, PC TAB	X1 - X10
3	7	ICN-163-S3G	ROBINSON NUGENT	SOCKET, DUAL IN-LINE (GOLD) 16-PIN	JC, JS, J2-J6
4	6	84-20-060-10	SOUTHCO	NO. 84 FRACTIONAL TURN FASTENER	
5				DELETED	
6	2	03-09-2052	MOLEX	CONNECTOR, RCPT, 5-CONTACT	J7,J8 (NOTE 1)
7	2	03-09-1052	MOLEX	CONNECTOR, PLUG, 5-CONTACT	(NOTE 1)
8	10	02-09-2133	MOLEX	PINS, CONNECTOR	(NOTE 2)
9	10	02-09-1118	MOLEX	SOCKETS, CONNECTOR	(NOTE 2)

NOTES

1. RECEPTACLE CONNECTOR J7 AND MATCHING PLUG CONNECTOR OPTIONAL PER SYSTEM REQUIREMENTS.
2. WHEN J7 IS NOT REQUIRE, QUANTITIES OF ITEMS 8 AND 9 ARE REDUCED TO 5 EACH.

TEST SET MODEM
PN 4110AC

FUNCTION

The Test Set modem printed circuit board (PCB) provides the FSK interface between the test set and the unit under test.

DESCRIPTION

The Modem is mounted on a 4½ x 6½ inch PCB. Interface with the mother board is through a dual 22-pin edge connector. Circuitry includes an asynchronous communication interface adapter (ACIA), peripheral interface adapter (PIA), modem, address comparator, programmable counter, amplifiers, gates, and two active audio filters. The PCB requires +5, +12, and -12 Vdc for operation.

THEORY OF OPERATION

The Modem PCB converts parallel digital data from the test set microprocessor logic into serial FSK data for application to the unit - under - test (UUT). (See block and logic diagrams.) Conversely, the modem also converts FSK data from the UUT into digital data for the test set microprocessor logic. The modem PCB also provides signals to front panel light-emitting diodes, (LED's) to produce visual indication of the transmit or receive function in process.

TRANSMIT. The digital data to be transmitted to the UUT enter the Modem PCB on the system data bus. The data are taken from the data bus by ACIA U11 when the R/W control signal is low and placed in ACIA registers. Next the data are serialized by internal shift registers and sent to modem U4 as TX DATA. This device converts the digital data into an FSK signal (TXCAR) which is applied to active bandpass transmit filter A1. The filter has its center frequency tuned for 1170 Hz if the test set is programmed as a Central Station, or 2125 Hz, if programmed as a Remote Station. Selection is accomplished by the PA7 signal from PIA U10. PA7 high selects 1170 Hz, and PA7 low selects 2125 Hz. The narrow passband characteristics of the filter pass a mark 100 Hz above, or a space 100 Hz below, the filter center frequency while blocking frequencies outside this spectrum.The filter output appears as signals DTA and DRA at the PCB edge connector pins 20 and Y.

RECEIVE. FSK signals received as DT and DR (pins X and 19) by the Test Set Modem PCB are converted into digital data by the same solid-state devices that provide the transmit conversion, except the process is reversed and filter A2 is used as the receive filter. This active circuit typically has its center frequency tuned for 2125 Hz if the test set is programmed as a Central Station, or 1170 Hz if programmed as a Remote Station. The center-frequency

selection process is similarly derived from signal PA7 with the gating logic providing the complement of the transmit-select logic gate. The receive circuitry additionally incorporates a squelch circuit (U9) that produces an output signal which is NANDed with the receive signal (U4-7) to inhibit noise from producing false data when no receive carrier is present.

PIA U10 also provides programmed ECHO, TYPE, and MODE selection signals (PA5, PA6, and PA7) for modem U4 in both the transmit and receive modes. The signals that drive PCB mounted LED's DS1 and DS2 (TX ON and RX ON) are connected to similar front panel LED's through drivers (U13). Two other signals (TX DATA and RX DATA) are also connected through drivers (U13) to front panel LED's.

Address decoder U6 generates the PCB enable signal (PDEN) when the bus address compares with the settings of switch S1. Programmable divider U8 is strapped for a 300 baud output which clocks the ACIA. The outputs of inverters U14 (PB5, CA1, PB7, PB6) are not used in the test set application.

ADJUSTMENTS

The Test Set Modem PCB contains three adjustment potentiometers; transmit level adjustment R17, receive level adjustment R25, and squelch level adjustment R16. (See logic diagram and parts location drawing.)

TRANSMIT LEVEL. Set the transmit level with the test equipment listed below, or equivalent, using the procedural steps that follow:

dB Meter	H-P 400H
Extender Board	ESI 4131AA

1. Install modem PCB on extender board.

2. Initiate a transmit data signal in the automatic mode at the test set front panel.

3. Connect dB meter and 75-ohm load to the test set TX audio leads (red and black wire pair in cable connected to test set INTERFACE connector).

4. Adjust transmit level potentiometer R17 for a reading on dB meter that conforms with the receive circuitry in the unit-under-test:

Controller Type	Level Required
4124AA	-15 dBm
4111AA	0 dBm

RECEIVE/SQUELCH LEVELS. Set the receive and squelch levels with the test equipment listed below, or equivalent, using the procedural steps that follow:

Audio Generator	H-P 200AB
Oscilloscope	H-P 1742A

1. Install modem PCB on extender board.

2. Connect audio generator to test set RX audio leads (green and white pair in cable connected to test set INTERFACE connector.)

3A. If test set is programmed as a Central Station, set audio generator for 0 dBm at 2125 Hz.

3B. If test set is programmed as a Remote Station, set audio generator for 0 dBm at 1170 Hz.

4. Connect oscilloscope between U2-4 (receive amplifier input) and PCB ground bus.

5. Adjust potentiometer R25 for a symmetrical sine wave at maximum level without clipping.

6. Move oscilloscope probe to amplifier output (U2-9) and check for square wave with 50-percent duty cycle. If necessary repeat step 5.

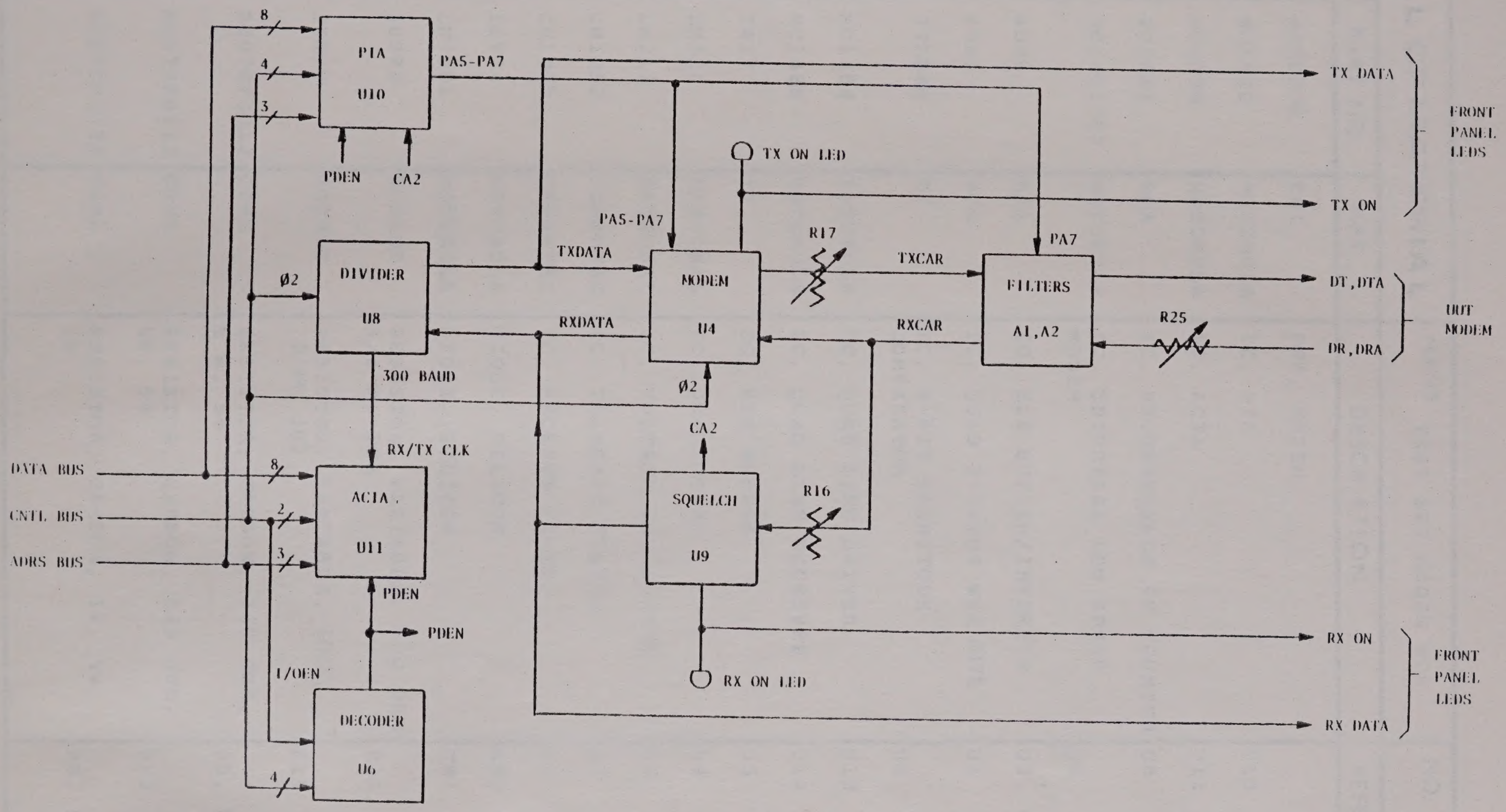
7. Disconnect oscilloscope.

8. Set audio generator output for -35 dBm.

9. Adjust squelch level potentiometer R16 until RX ON indicator on test set front panel just goes out.

PARTS LIST

The Test Set Modem PCB parts are listed in the Bill of Material. A parts location drawing appears following the Bill of Material.


PIA
U10
PA5-PA7
PDEN
CA2
8
4
3
DIVIDER
U8
Ø2
300 BAUD
TXDATA
RXDATA
PA5-PA7
MODEM
U4
Ø2
TX ON LED
R17
TXCAR
RXCAR
PA7
FILTERS
A1,A2
R25
TX DATA
TX ON
FRONT PANEL LEDS
DT,DTA
DR,DRA
UUT MODEM
DATA BUS
CNTL BUS
ADRS BUS
8
2
3
ACIA
U11
RX/TX CLK
PDEN
PDEN
I/OEN
DECODER
U6
4
CA2
SQUELCH
U9
R16
RX ON LED
RX ON
RX DATA
FRONT PANEL LEDS

Test Set Modem PCB Block Diagram

BILL OF MATERIAL	NAME TEST SET MODEM PCB	NO. BM4110AC02

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4110AA00	ESI	PWB, MODEM	
2	1	MC6820	MOTOROLA	IC, PIA	U10
3	1	MC6850	MOTOROLA	IC, ACIA	U11
4	1	4059AE	RCA	IC, PROGRAMMABLE ÷N COUNTER	U8
5	1	MC14412FP	MOTOROLA	IC, UNIVERSAL LOW SPEED MODEM	U4
6	2	4049	RCA	IC, HEX BUFFER/INVERTER	U3, U12
7	1	4001	RCA	IC, QUAD 2-INPUT NOR GATE	U1
8	1	74LS85	TI	IC, 4-BIT MAGNITUDE COMPARATOR	U6
9	1	MC1488	MOTOROLA	IC, QUAD LINE DRIVER	U13
10	1	MC1489	MOTOROLA	IC, QUAD LINE RECEIVER	U14
11	1	7417	TI	IC, HEX BUFFER	U5
12	1	LM324	NATIONAL	IC, QUAD OPAMP	U9
13	1	LM211	NATIONAL	IC, VOLTAGE COMPARATOR	U2
14	1	CH1252	CERMETEK	IC, TRANSMIT FILTER	A1
15	1	CH1257	CERMETEK	IC, RECEIVE FILTER	A2
16	5	1N914	MOTOROLA	DIODE, SILICON	CR3 - CR7
17	2	1N4001	MOTOROLA	DIODE, SILICON	CR1, CR2
18	2	3009P	BOURNS	RESISTOR, VARIABLE, 500 OHMS 3/4 W, 10%	R16, R25
19	1	3009P	BOURNS	RESISTOR, VARIABLE, 100K, 3/4W, 10%	R17
20	2	RC07GF331J	COML	RESISTOR, CARBON, 330 OHM, ¼ W, 5%	R5, R6
21	2	RC07GF621J	COML	RESISTOR, CARBON, 620 OHM, ¼W, 5%	R23, R24
22	3	RC07GF102J	COML	RESISTOR, CARBON, 1K, ¼W, 5%	R9, R13, R15

BILL OF MATERIAL

NAME TEST SET MODEM PCB

NO. BM4110AC02

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
23	1	RC07GF222J	COML	RESISTOR, CARBON 2.2K, ¼W, 5%	R10
24	4	RC07GF332J	COML	RESISTOR, CARBON 3.3K, ¼W, 5%	R1 THRU R4
25	2	RN55C1002F	COML	RESISTOR, FILM, 10K, ¼W, 1%	R21, R22
26	3	RC07GF103J	COML	RESISTOR, CARBON, 10K, ¼W, 5%	R12, R14, R18
27	2	RC07GF104J	COML	RESISTOR, CARBON, 100K, ¼W, 5%	R19, R20
28	1	RC07GF154J	COML	RESISTOR, CARBON, 150K, ¼W, 5%	R11
29	4	DD-331	CENTRALAB	CAPACITOR, CERAMIC, 330 pF, 1KV, 10%	C11, C12, C13, C14
30	1	UK25-503	CENTRALAB	CAPACITOR, CERAMIC, 0.05uF 25V, 20%	C6
31	3	UK12-104	CENTRALAB	CAPACITOR, CERAMIC, 0.1uF 12 V, 20%	C4, C5 C10
32				DELETED	
33	1	WMF05P22	CORNELL-DUBILIER	CAPACITOR, FILM, 0.22 uF, 50V, 10%	C8
34	1	13F105KL	SPRAGUE	CAPACITOR, TANTALUM, 1.0uF, 35V, 10%	C9
35	3	150D225X9020A	SPRAGUE	CAPACITOR, TANTALUM, 2.2 uF, 20V, 20%	C1, C2, C3
36	2	SP-67	TRIAD	TRANSFORMER, 600-OHM CENTER TAP	T1, T2
37	1	206-4	CTS	SWITCH, SPST, DIP	S1 - S4
38	2	550-0103	DIALCO	LED, RED (WITH HOLDER)	DS1, DS2
39	1	ICN406S4G	ROBINSON NUGENT	SOCKET, 40-PIN DIP	XU10

BILL OF MATERIAL				NAME TEST SET MODEM PCB	NO. BM4110AC02
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
40	2	ICN246S4G	ROBINSON NUGENT	SOCKET, 24-PIN DIP	XU8,XU11
41	1	ICN163S3G	ROBINSON NUGENT	SOCKET, 16-PIN DIP	XU4
42	1	ICN143S3G	ROBINSON NUGENT	SOCKET, 14-PIN DIP	XU2
43	2	NPN	ESI	SOCKET, 16 PIN, SPECIAL LOCAL MFG--USE RN ICN246S4G AND CUT OFF PORTION OF DIP NOT NEEDED.	XA1, XA2

NOTES:

1. XU7 CONSISTS OF 16-PIN DIP PADS ONLY.

2. CUT LANDS AS FOLLOWS:

FROM	TO
U13-4&5	U10-6
U13-9&10	U10-14
U13-12&13	U10-5

3. INSTALL JUMPERS AS FOLLOWS:

FROM	TO
U1-1&2	U1-7
U13-4&5	U12-12
U13-9&10	U3-15
U13-12&13	U11-6
XU7-11	U12-10

4 R24 & T2 NOT INSTALLED ON 2-WIRE SYSTEMS.

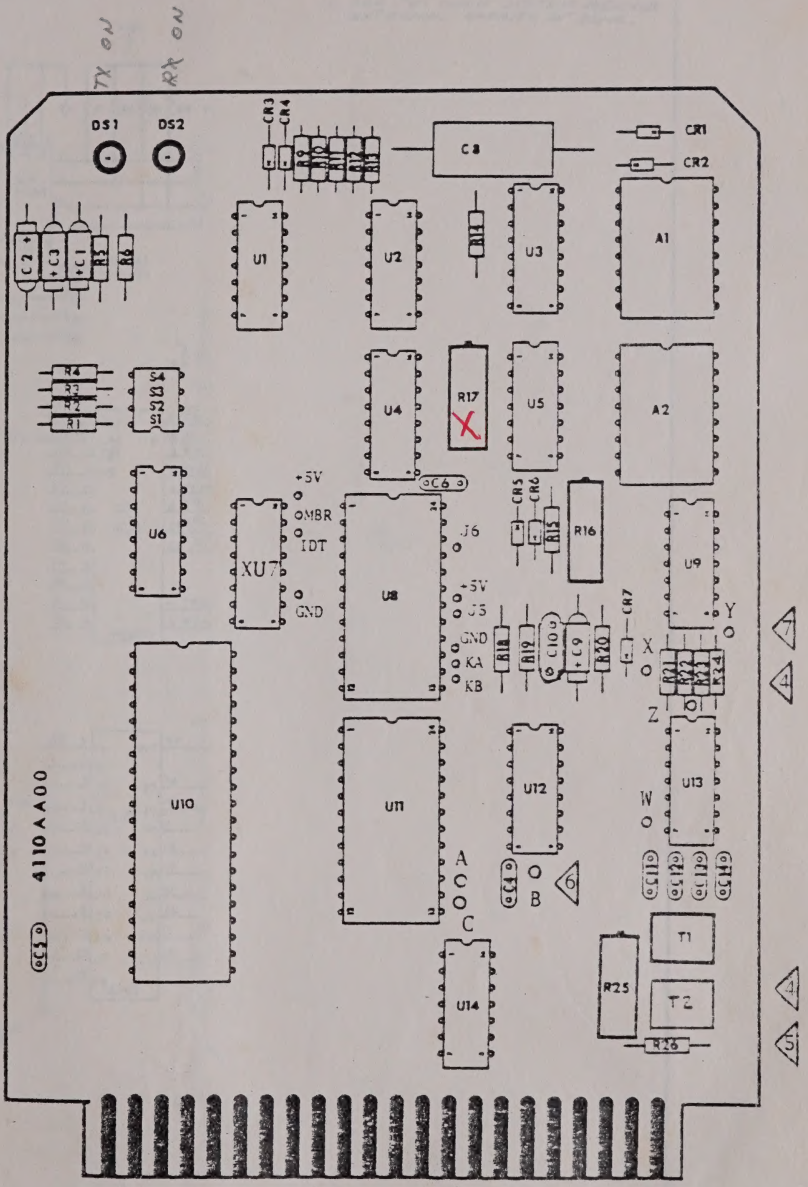
5 R26 INSTALLED FOR IMPEDANCE MATCH ONLY IF SYSTEM IMPEDANCE IS LESS THAN 600 OHMS.

6 IF SYSTEM REQUIRES $\overline{\text{DCD}}$ INPUT TO ACIA, JUMPER:

U12-7(A) TO U12-10(B)

IF $\overline{\text{DCD}}$ NOT REQUIRED, JUMPER:

U12-7(A) TO +5V(C)

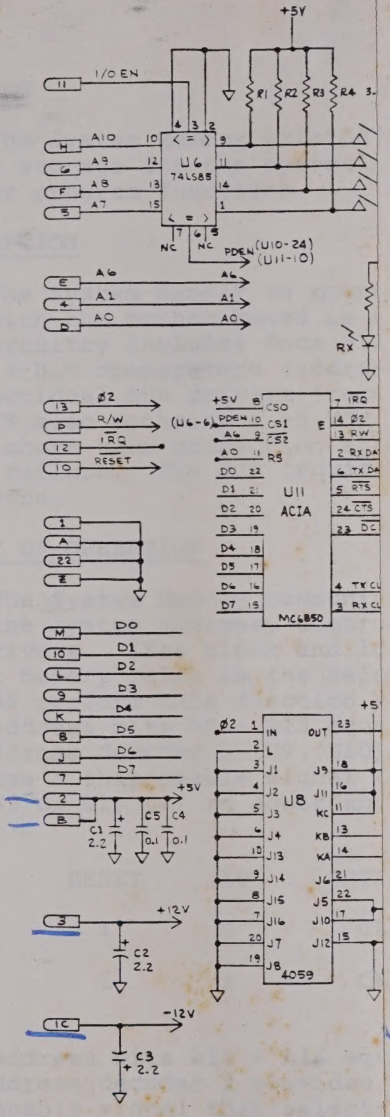

TX ON
RX ON
DS1
DS2
CR3
CR4
C8
CR1
CR2
C2
C3
C1
R5
R6
R14
U1
U2
U3
A1
R4
R3
R2
R1
S4
S3
S2
S1
U4
R17
U5
A2
C6
+5V
MBR
IDT
GND
U6
XU7
U8
J6
+5V
J5
GND
KA
KB
CR5
CR6
R15
R16
U9
CR7
R18
R19
C10
C9
R20
X
Y
R21
R22
R23
R24
Z
4110AA00
U10
U11
U12
U13
W
A
B
C
C4
C11
C12
C13
C14
C5
T1
T2
R25
R26
U14
7
4
4
5
6

7 FOR 4-WIRE SYSTEM, CUT X TO Z LAND AND JUMPER:

A1-3(X) TO T2-6(Y)

R22/R23 JCT(Z) TO GND(W)

Test Set Modem PCB Parts Location


+5V
I/O EN
11
H
6
F
5
A10
A9
A8
A7
U6
74LS85
R1
R2
R3
R4
3.
NC
PDEN
(U10-24)
(U11-10)
E
4
D
A6
A1
A0
RX
13
P
12
10
Ø2
R/W
IRQ
RESET
+5V
(U6-6)
PDEN
CS0
CS1
CS2
RS
D0
D1
D2
D3
D4
D5
D6
D7
U11
ACIA
MC6850
E
IRQ
Ø2
RW
RX DA
TX DA
RTS
CTS
DC
TX CL
RX CL
1
A
22
Z
M
10
L
9
K
8
J
7
2
B
D0
D1
D2
D3
D4
D5
D6
D7
+5V
C1
2.2
C5
0.1
C4
0.1
3
+12V
C2
2.2
1C
-12V
C3
2.2
Ø2
IN
OUT
L
J1
J2
J3
J4
J13
J14
J15
J16
J7
J8
U8
4059
J9
J11
KC
KB
KA
J6
J5
J10
J12
+5
ON

NOTES CONT:

11. ADD JW1 WHEN SYSTEM REQUIRES EXTERNAL "CARRIER ON" SIGNAL.

REV	BY	DESCRIPTION	DATE	APPROVED
03	RC	ADD "CARR ON" JMPR (A095)	12/20/	
02	DF	CHG RXD & SQRX (A084)	11/13 8	
01	KJF	CHG REF DES (A079)	[illegible]	

REVISIONS

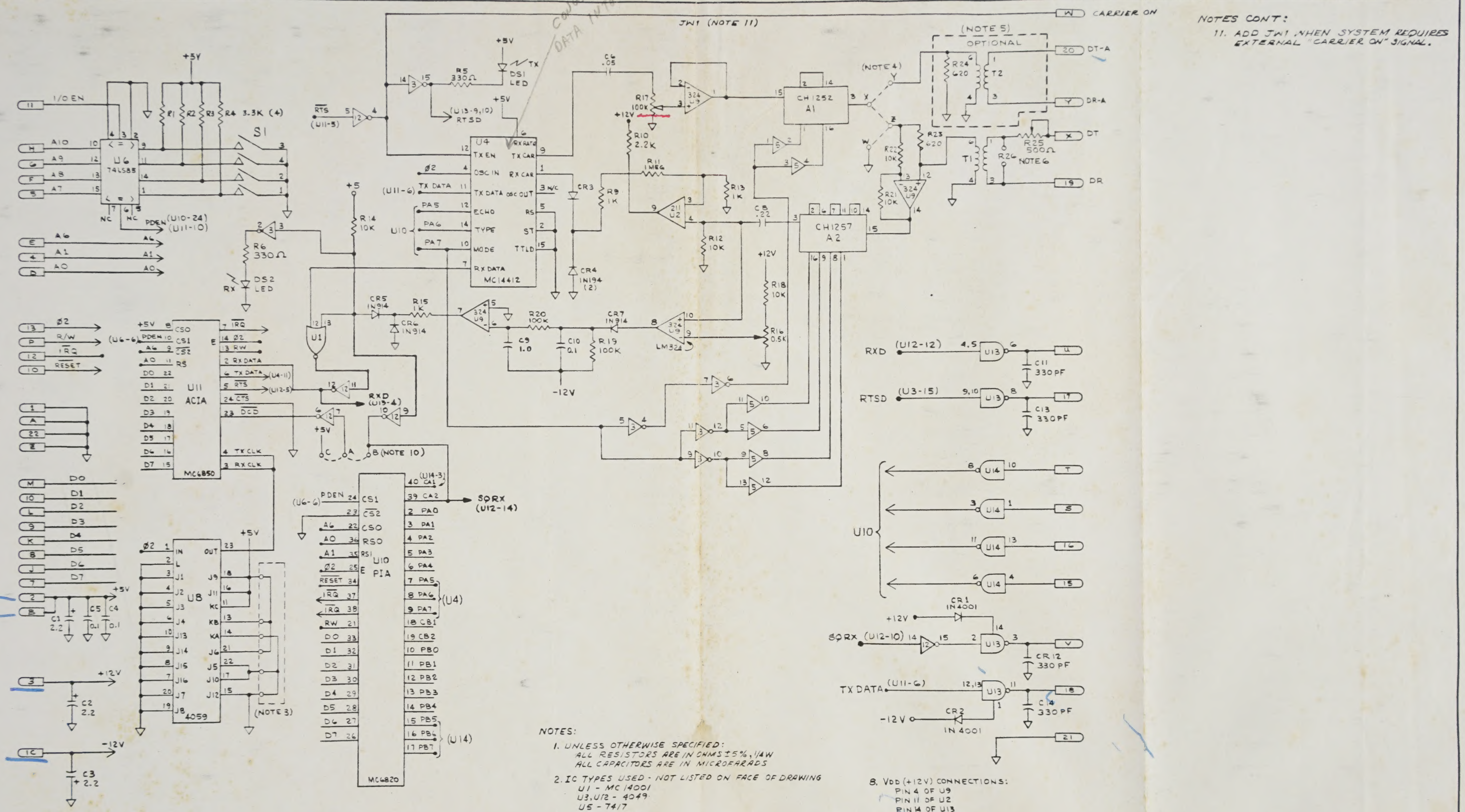
DR [illegible] 3/10/78

TITLE LOGIC DIAGRAM – MODEM, TEST SET CENTRAL/ REMOTE

ISSUE 03

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA

DWG NO LD4110AC


CONVERTS DIGITAL DATA INTO TX CARRIER
JW1 (NOTE 11)
CARRIER ON
I/O EN
A10
A9
A8
A7
A6
A1
A0
U6
74LS85
R1 R2 R3 R4 3.3K (4)
S1
+5V
RTS (U11-5)
R5 330Ω
DS1 LED
TX
(U13-9,10) RTSD
U4
TX EN
OSC IN
TX DATA
ECHO
TYPE
MODE
RX DATA
MC14412
RX RATE
TX CAR
RX CAR
OSC OUT
RS
ST
TTLD
(U11-6) TX DATA
PA5
PA6
PA7
U10
R14 10K
R6 330Ω
DS2 LED
RX
C6 .05
R17 100K
+12V
R10 2.2K
R11 1MEG
R9 1K
R13 1K
CR3
CR4 IN194 (2)
R12 10K
C8 .22
324 U9
211 U2
CH1252 A1
CH1257 A2
(NOTE 5) OPTIONAL
(NOTE 4)
R24 620
T2
DT-A
DR-A
DT
DR
R22 10K
R23 620
R21 10K
T1
R25 500Ω
R26
NOTE 6
R18 10K
R16 0.5K
CR5 IN914
R15 1K
CR6 IN914
R20 100K
C9 1.0
C10 0.1
R19 100K
CR7 IN914
LM324
-12V
U1
φ2
R/W
IRQ
RESET
U11 ACIA
MC6850
CS0
CS1
CS2
RS
D0 D1 D2 D3 D4 D5 D6 D7
TX CLK
RX CLK
DCD
CTS
RXD (U13-4)
B (NOTE 10)
U8
4059
C1 2.2
C5 0.1
C4 0.1
C2 2.2
C3 2.2
(NOTE 3)
PDEN
U10 PIA
MC6820
CA1
CA2
SQRX (U12-14)
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7
CB1 CB2
PB0 PB1 PB2 PB3 PB4 PB5 PB6 PB7
(U4)
(U14)
RXD (U12-12)
RTSD (U3-15)
U13
C11 330PF
C13 330PF
U14
CR1 IN4001
SQRX (U12-10)
CR12 330 PF
TX DATA (U11-6)
CR2 IN 4001
C14 330 PF

NOTES CONT:

11. ADD JW1 WHEN SYSTEM REQUIRES EXTERNAL "CARRIER ON" SIGNAL.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS ±5%, 1/4W
   ALL CAPACITORS ARE IN MICROFARADS
2. IC TYPES USED - NOT LISTED ON FACE OF DRAWING
   U1 - MC 14001
   U3, U12 - 4049
   U5 - 7417
   U13 - MC 1488
   U14 - MC 1489
3. 300 BAUD JUMPERS SHOWN.
4. JUMPER X TO Y AND W TO Z FOR 4 WIRE SYSTEM REQUIREMENTS.
5. INSTALL XMFR T2 FOR 4 WIRE APPLICATIONS ONLY
6. R26 IS OPTIONAL. USE TO MATCH IMPEDANCE IF LINE IS LESS THAN 600Ω
7. Vcc (+5V) CONNECTIONS:
   PIN 1 OF U3, U12
   PIN 12 OF U11
   PIN 14 OF U1, U5, U14
   PIN 16 OF U4, U6
   PIN 20 OF U10
   PIN 24 OF U8
8. VDD (+12V) CONNECTIONS:
   PIN 4 OF U9
   PIN 11 OF U2
   PIN 14 OF U13

   VEE (-12V) CONNECTIONS:
   PIN 1 OF U13
   PIN 2 OF U2
   PIN 11 OF U9
9. VSS (GND) CONNECTIONS:
   PIN 1 OF U10, U11
   PIN 7 OF U1, U4, U13, U14
   PIN 8 OF U3, U4, U12
   PIN 12 OF U8
   PIN 1 AND 2 OF U1
10. JUMPER A TO B WHEN ACIA INPUT DATA CARRIER DETECT (DCD) IS REQUIRED. IF NOT REQUIRED, JUMPER A TO C.

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO ENGINEERED SYSTEMS, INC AND SHALL NOT BE USED FOR ENGINEERING, DESIGN, PROCUREMENT, OR MANUFACTURE IN WHOLE OR IN PART WITHOUT CONSENT OF ENGINEERED SYSTEMS, INC.

REV	BY	DESCRIPTION	DATE	APPROVED
03	RC	ADD "CARR ON" JMPR (A095)	12/20/9	
02	DF	CHG RXD & SQRX (A084)	[illegible]	
01	[illegible]	CHG REF DES (A079)	[illegible]	

REVISIONS

DR 3/10/78

ISSUE 03

TITLE LOGIC DIAGRAM - MODEM, TEST SET CENTRAL/ REMOTE

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA

DWG NO LD4110AC

FUNCTION

The System Memory printed circuit board (PCB) provides permanent storage for the operating system (OS) and temporary storage for program functions.

DESCRIPTION

The System Memory is mounted on a 4½ x 6½ inch PCB. Interface with the mother board is through a dual 22-pin edge connector. The circuitry includes four 512 x 8 PROM's four 256 x 4 RAM's, three 4-bit comparators (address decoders), two 4-bit parallel bidirectional bus drivers (receiver/driver), and gating circuits. The PCB also contains a +5 Vdc nickel-cadmium battery that provides short-term protection against loss of stored data due to power failure. The PCB requires +5 and +12 volts dc for normal operation.

THEORY OF OPERATION

The System Memory communicates only with the System Controller over the system address, control, and data buses via TTL receivers and drivers. (See block and logic diagrams.) Address bits A0 - A7 select memory cells in the selected RAM (U1 - U4); address bits A0 - A8 perform this function for the selected PROM (U5 - U8). When address bits A9 - A15 equal the binary code setting (Appendix A), address decoder 1 (U9, U10) provides PDEN 1 to gate 1 which produces a chip-enable signal that selects a 256 x 8 RAM pair (U1, U3 or U2, U4) in accordance with the following truth table.

PDEN1	RESET	A8	OUTPUT	ENABLE
1	1	0	CE-0	U1, U3
1	1	1	CE-1	U2, U4

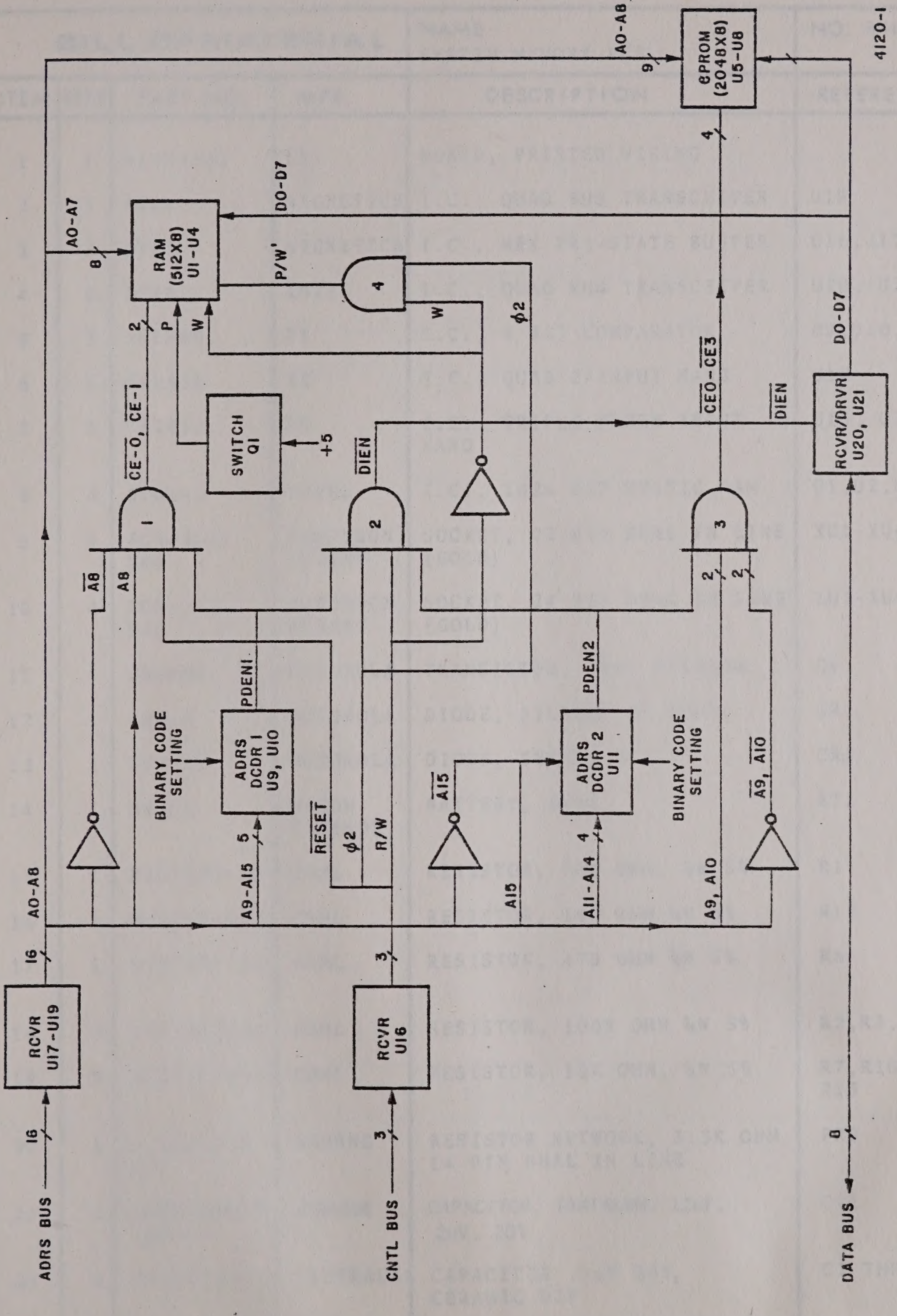
when address bits A11 - A14 equal the binary code setting (Appendix A), address decoder 2 provides PDEN 2 to gate 3 which produces a chip-enable signal that selects a 1024 x 8 PROM (U5 - U8) in accordance with the following truth table:

PDEN2	A10	A9	OUTPUT	ENABLE
1	0	0	CEO	U5
1	0	1	CE1	U6
1	1	0	CE2	U7
1	1	1	CE3	U8

PDEN2 also enables gate 2 which, if RESET is high, translates the R/W control signal into a data directional control signal for receiver/driver U20, U21 ($\overline{\text{DIEN}}$ = data in, DIEN = data out). The R/W signal is also clocked (Ø2) through gate 4 to control the RAM read or write cycle (R/W = read, $\overline{\text{R/W}}$ = write). The R/W signal is also inverted and applied to the RAM's to disable their output functions during a read cycle. The transistor switch disables the RAM's if the +5 Vdc drops.

PARTS LIST

The System Memory parts are listed in the Bill of Material. A parts location drawing appears following the Bill of Material.


ADRS BUS
16
RCVR U17-U19
16
A0-A8
CNTL BUS
3
RCVR U16
3
DATA BUS
8
A0-A7
8
RAM (512X8) U1-U4
D0-D7
P/W'
2
P
W
CE-0, CE-1
SWITCH Q1
+5
4
W
φ2
DIEN
1
2
3
A8
A8
PDEN1
BINARY CODE SETTING
ADRS DCDR 1 U9, U10
5
A9-A15
RESET
φ2
R/W
A15
A15
PDEN2
ADRS DCDR 2 U11
4
A11-A14
BINARY CODE SETTING
A9, A10
A9, A10
2
2
CE0-CE3
DIEN
RCVR/DRVR U20, U21
D0-D7
4
EPROM (2048X8) U5-U8
9
A0-A8
4120-1

System Memory PCB Block Diagram

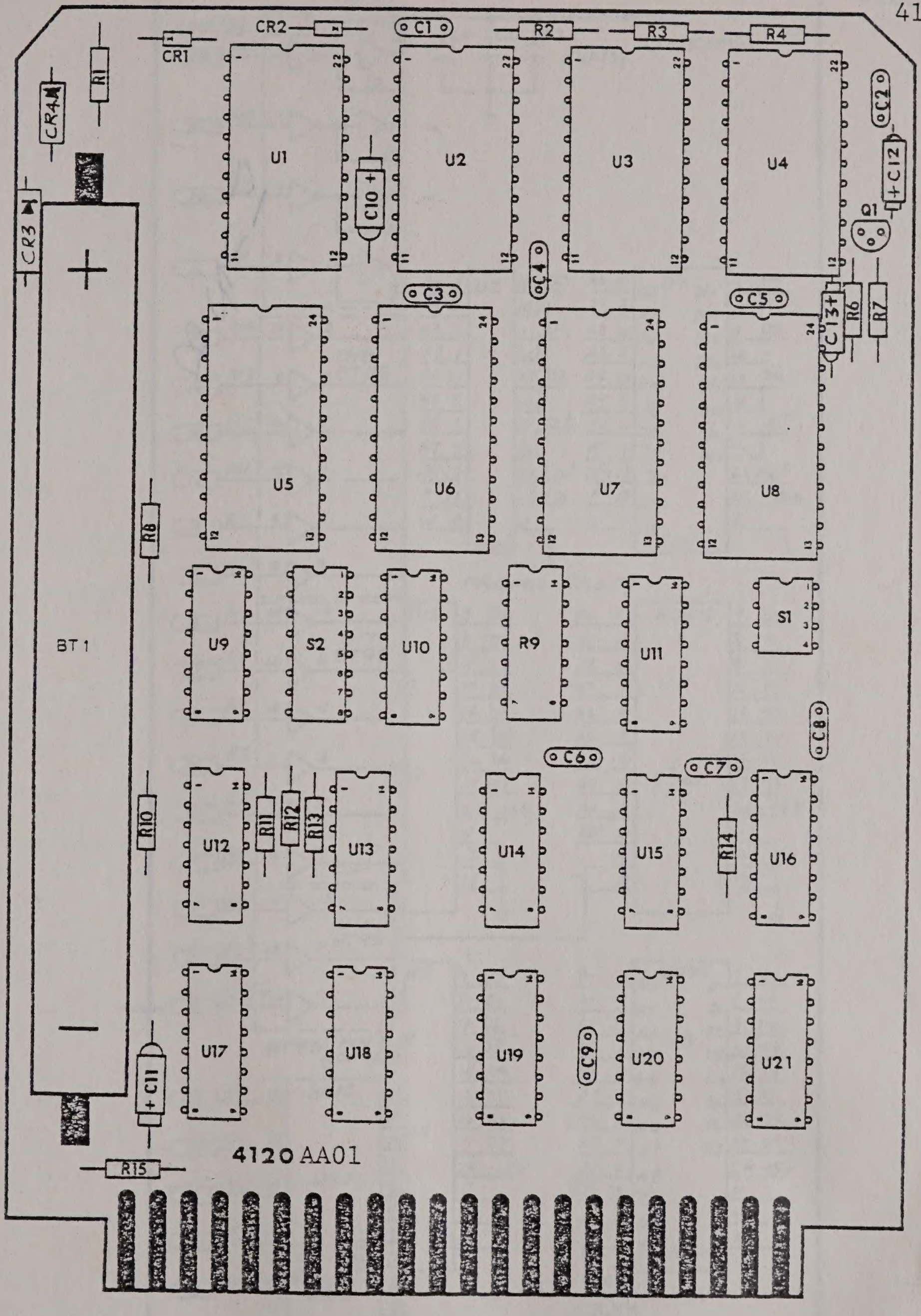
BILL OF MATERIAL	NAME SYSTEM MEMORY PCB	NO. BM4120AA04

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4120AA01	ESI	BOARD, PRINTED WIRING	
2	1	8T26	SIGNETICS	I.C., QUAD BUS TRANSCEIVER	U19
3	3	8T95	SIGNETICS	I.C., HEX TRI-STATE BUFFER	U16,U17,U18
4	2	8216	INTEL	I.C., QUAD BUS TRANSCEIVER	U20, U21
5	3	74LS85	TI	I.C., 4 BIT COMPARATOR	U9,U10,U11
6	1	74LS00	TI	I.C., QUAD 2-INPUT NAND	U12
7	3	74LS10	TI	I.C., TRIPLE THREE INPUT NAND	U13, U14, U15
8	4	5101-1	INTEL	I.C., 1024 BIT STATIC RAM	U1,U2,U3,U4
9	4	ICN-224-S4G	ROBINSON NUGENT	SOCKET, 22 PIN DUAL IN LINE (GOLD)	XU1-XU4
10	4	ICN-246-S4G	ROBINSON NUGENT	SOCKET, 24 PIN DUAL IN LINE (GOLD)	XU5-XU8
11	1	2N3906	MOTOROLA	TRANSISTOR, PNP, SILICON	Q1
12	1	1N914	MOTOROLA	DIODE, SILICON OR EQUIV.	CR2
13	1	1N4735	MOTOROLA	DIODE, ZENER, 6.2V	CR1
14	1	N4326	UNION CARBIDE	BATTERY, 5VDC	BT1
15	1	RC07GF101J	COML	RESISTOR, 100 OHM, ¼W 5%	R1
16	1	RC07GF161J	COML	RESISTOR, 160 OHM ¼W 5%	R15
17	1	RC07GF471J	COML	RESISTOR, 470 OHM ¼W 5%	R6
18	3	RC07GF104J	COML	RESISTOR, 100K OHM ¼W 5%	R2,R3,R4
19	5	RC07GF103J	COML	RESISTOR, 10K OHM, ¼W 5%	R7,R10,R11,R12 R13
20	1	4114R-002 332	BOURNS	RESISTOR NETWORK, 3.3K OHM, 14 PIN DUAL IN LINE	PR9
21	1	196D126X9020 JA1	SPRAGUE	CAPACITOR, TANTALUM, 12uF, 20V, 20%	C11
22	9	CY20C104M	CENTRALAB	CAPACITOR .1uF 50V, CERAMIC DIP	C1 THRU C9

BILL OF MATERIAL				NAME SYSTEM MEMORY PCB	NO. BM4120AA04
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
23	2	RC07GF332J	COML	RESISTOR, CARBON, 3.3K, ¼W, 5%	R8,R14
24	2	1N4001	MOTOROLA	DIODE	CR3,CR4
25	2	D222Y15M	SIEMENS	CAPACITOR, 22 uF, 15V	C10,C12
26	1	CT22504	CENTRALAB	CAPACITOR, 2.2 uF, 16V	C13
27	REF	82S115	SIGNETICS	PROM, 2048 BIT	U5,U6,U7,U8 (NOTE 1)
28	1	206-4	CTS	SWITCH, DIP, 4-SPDT	S1
29	1	206-8	CTS	SWITCH, DIP, 8-SPDT	S2

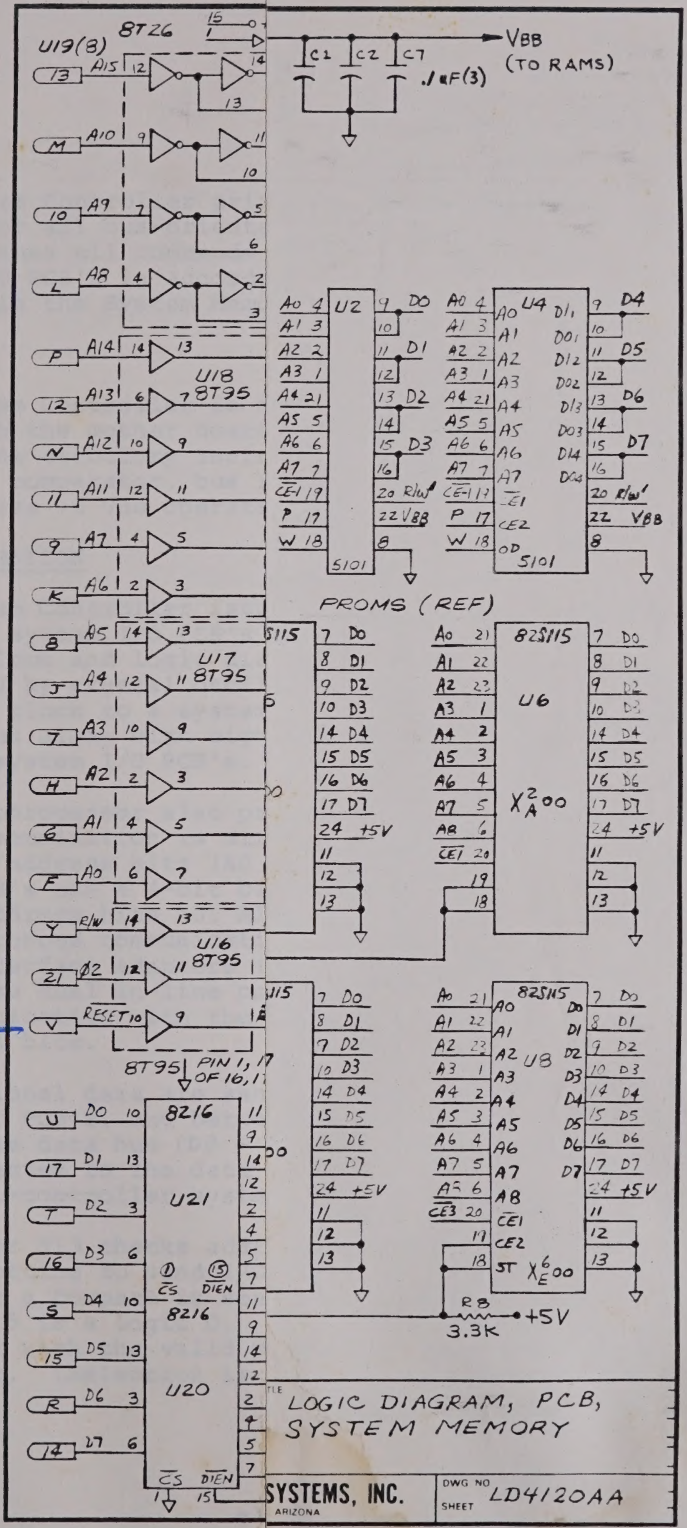
NOTES

1. SEE SYSTEM BILL OF MATERIALS FOR PROM QUANTITIES.

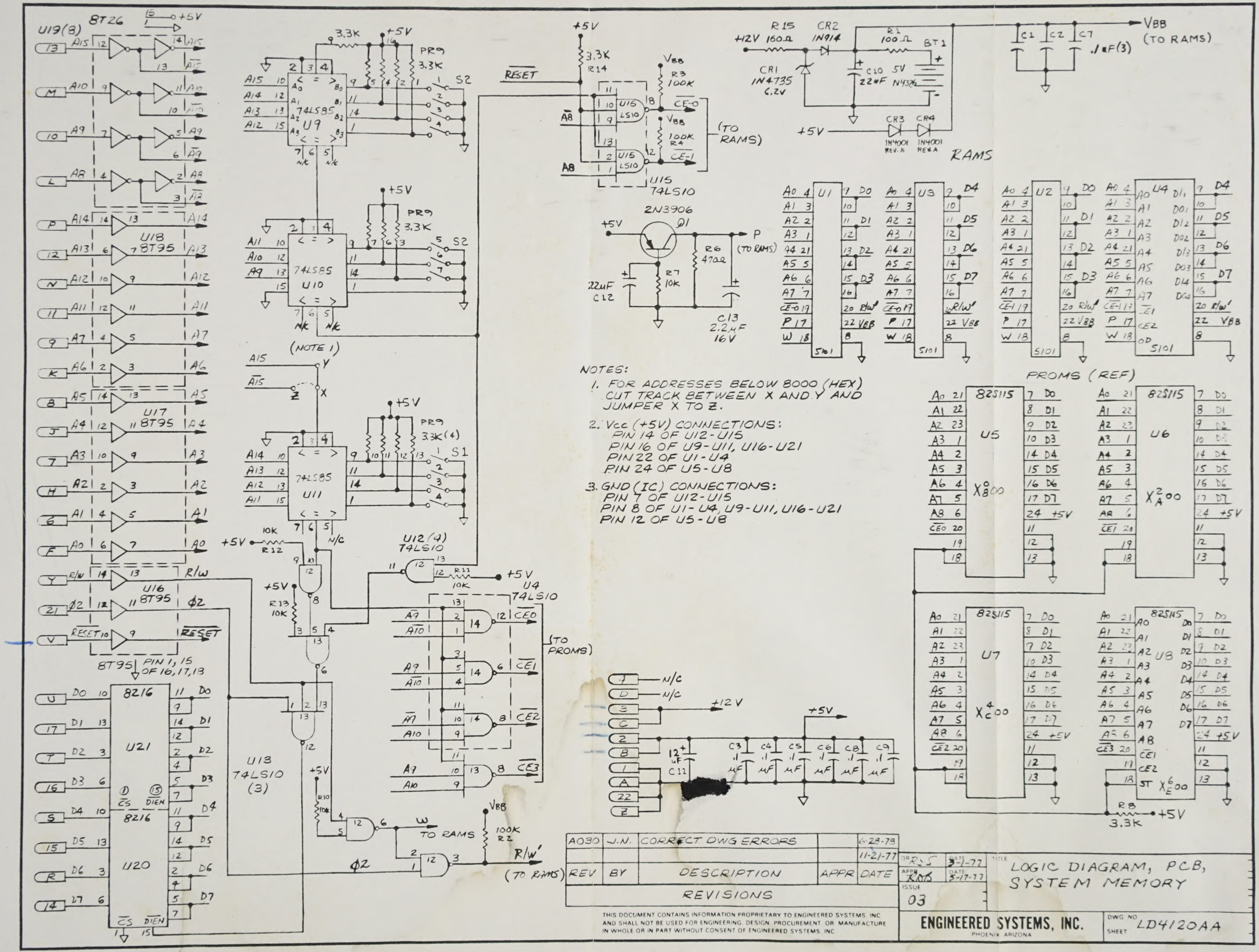

CR1
CR2
C1
R2
R3
R4
R1
CR4
CR3
U1
U2
U3
U4
C10
C2
C12
Q1
C3
C4
C5
C13
R6
R7
U5
U6
U7
U8
R8
U9
S2
U10
R9
U11
S1
BT1
C8
C6
C7
R10
U12
R11
R12
R13
U13
U14
U15
R14
U16
U17
U18
U19
C9
U20
U21
C11
R15
4120 AA01

System Memory PCB Parts Location

14VZB


U19(8)
8T26
VBB (TO RAMS)
C1 C2 C7 .1uF(3)
A15 A10 A9 A8
A14 A13 A12 A11 A7 A6
U18 8T95
A5 A4 A3 A2 A1 A0
U17 8T95
R/W Ø2 RESET
U16 8T95
8T95 PIN 1, 17 OF 16, 17
U2 5101
U4 5101
D0 D1 D2 D3 D4 D5 D6 D7
R/W' VBB
PROMS (REF)
82S115
U6
$X_A^2 00$
U8
$X_E^6 00$
+5V
R8 3.3K
8216 U21
8216 U20
CS DIEN
LOGIC DIAGRAM, PCB, SYSTEM MEMORY
SYSTEMS, INC.
ARIZONA
DWG NO
SHEET
LD4120AA

14V2B


U19(8)
8T26
+5V
A15
A10
A9
A8
U18
8T95
U17
8T95
U16
8T95
PIN 1, 15 OF 16, 17, 18
8T95
RESET
R/W
ϕ2
8216
U21
U20
CS
DIEN
74LS85
U9
U10
U11
PR9
3.3K
3.3K(4)
S1
S2
N/C
(NOTE 1)
X
Y
Z
U12(4)
74LS10
U13
74LS10
(3)
U14
74LS10
R11
10K
R12
10K
R13
10K
R10
10K
W
TO RAMS
R/W'
(TO RAMS)
VBB
100K
R2
CE0
CE1
CE2
CE3
(TO PROMS)
R14
3.3K
U15
LS10
74LS10
A8
CE-0
CE-1
R3
100K
R4
100K
(TO RAMS)
2N3906
Q1
R6
470Ω
R7
10K
C12
22uF
C13
2.2uF
16V
P
(TO RAMS)
+12V
R15
160Ω
CR2
1N914
CR1
1N4735
6.2V
R1
100Ω
BT1
C10
22uF
5V
N4326
CR3
CR4
1N4001
REV. A
VBB
(TO RAMS)
C1
C2
C7
.1uF(3)
RAMS
U1
U2
U3
U4
5101
PROMS (REF)
82S115
U5
U6
U7
U8
X800
XA200
XC400
XE600
R8
3.3K
C11
12uF
C3
C4
C5
C6
C8
C9
.1uF

NOTES:

1. FOR ADDRESSES BELOW 8000 (HEX) CUT TRACK BETWEEN X AND Y AND JUMPER X TO Z.

2. Vcc (+5V) CONNECTIONS:
PIN 14 OF U12-U15
PIN 16 OF U9-U11, U16-U21
PIN 22 OF U1-U4
PIN 24 OF U5-U8

3. GND (IC) CONNECTIONS:
PIN 7 OF U12-U15
PIN 8 OF U1-U4, U9-U11, U16-U21
PIN 12 OF U5-U8

REV	BY	DESCRIPTION	APPR	DATE
A030	J.N.	CORRECT DWG ERRORS		6-28-78
				11-21-77

REVISIONS

DR R.S.S DATE 3-1-77
APPR KDB DATE 5-17-77
ISSUE 03

TITLE LOGIC DIAGRAM, PCB, SYSTEM MEMORY

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA

DWG NO LD4120AA
SHEET

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FUNCTION

The System Controller printed circuit board (PCB) is the control center for all bus-oriented system I/O PCB's. The System Controller issues all commands and processes all data to and from the system I/O PCB's in accordance with the system program (software) stored in the System Memory.

DESCRIPTION

The System Controller is mounted on a 4½ x 6½ inch PCB. Interface with the mother board is through a dual 22-pin edge connector. The circuitry includes a microprocessor, crystal oscillator, timer, comparator, bus receiver/drivers, and reset circuit. The PCB requires +5 Vdc operating voltage.

THEORY OF OPERATION

The System Controller issues all commands to and processes data from the system I/O PCB's under direction of the system program. (See block and logic diagrams.) Clocking for microprocessor U9 is provided by crystal oscillator Y1 at 4 MHz. The microprocessor converts this clock to a system clock of 1 MHz that is placed on the control bus along with eight other control signals for the bus-oriented system I/O PCB's.

The microprocessor also provides the address of the I/O PCB with which communication is directed by the system program by placing coded address bits (A0 - A15) on the address bus. All system I/O PCB's use a 4-bit binary code (A7 through A10) as their addresses. Address bits A0, A1, and A6 from the System Controller select asynchronous communication interface adapters (ACIA) and peripheral interface adapters (PIA) and registers internally contained in these dual in-line packages (DIP's) on the system I/O PCB's. Communication with the System Memory, however, required all 16 address bits.

Bidirectional data are sent between the microprocessor and the system I/O PCB's, and between the microprocessor and System Memory, via the data bus (D0 - D7). An 8-bit DIP switch (S1 - S8) which is connected to the data bus, can be used for maintenance or, in a multi-controller system for controller identification.

Comparator U13 checks address bits A11 through A14 with its binary code setting to send I/OEN on the control bus to the system I/O PCB's when a compare is sensed. I/OEN will be inhibited if address bit A15 is a logic 0. In some systems, address bit A15 will be AND'ed with the valid memory address (VMA) output of the microprocessor. (Selection is by optional jumpering.)

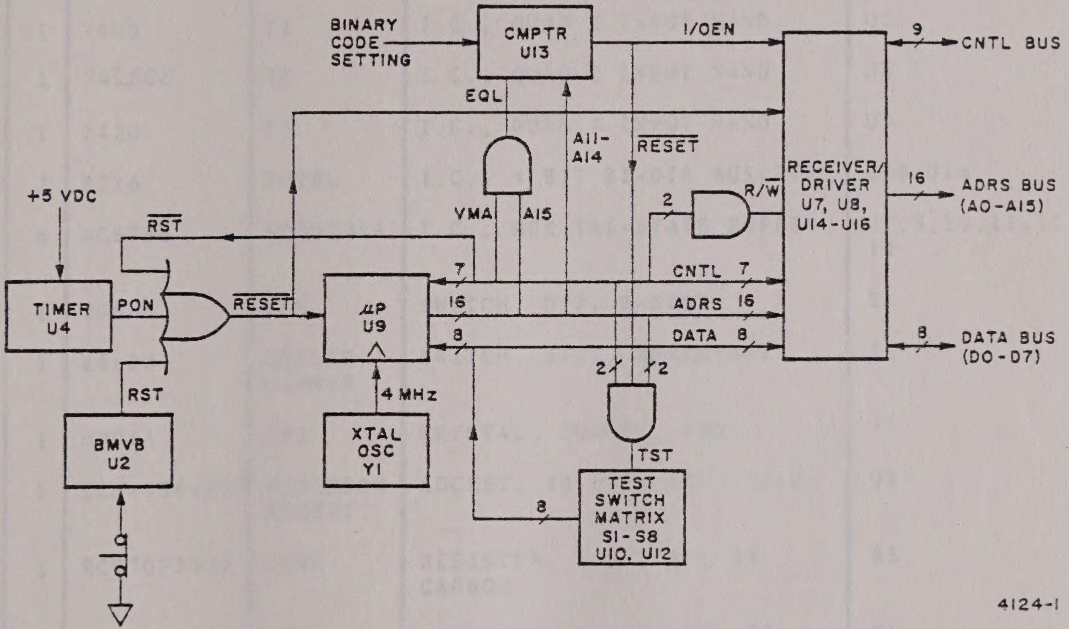
The System Controller sends up to five signals to the system I/O PCB's and receives up to four signals in return from the system I/O PCB's on the control bus. These signals are defined as follows:

MNEMONIC	NAME
TO SYSTEM CONTROLLER	
HALT	HALT
IRQ	Interrupt request
NMT	Nonmaskable interrupt request
RST	Reset microprocessor
FROM SYSTEM CONTROLLER	
Ø2	1MHz clock
BA	Bus available
I/OEN	Input/output enable
R/W	Read or write enable
RESET	Reset I/O PCB registers

The reset circuit is used during a power-up function via timer U4 to place the microprocessor in the start condition and also to clear registers in the system I/O PCB's. A momentary-open toggle switch on the PCB can be used to initiate the reset function during maintenance.

PARTS LIST

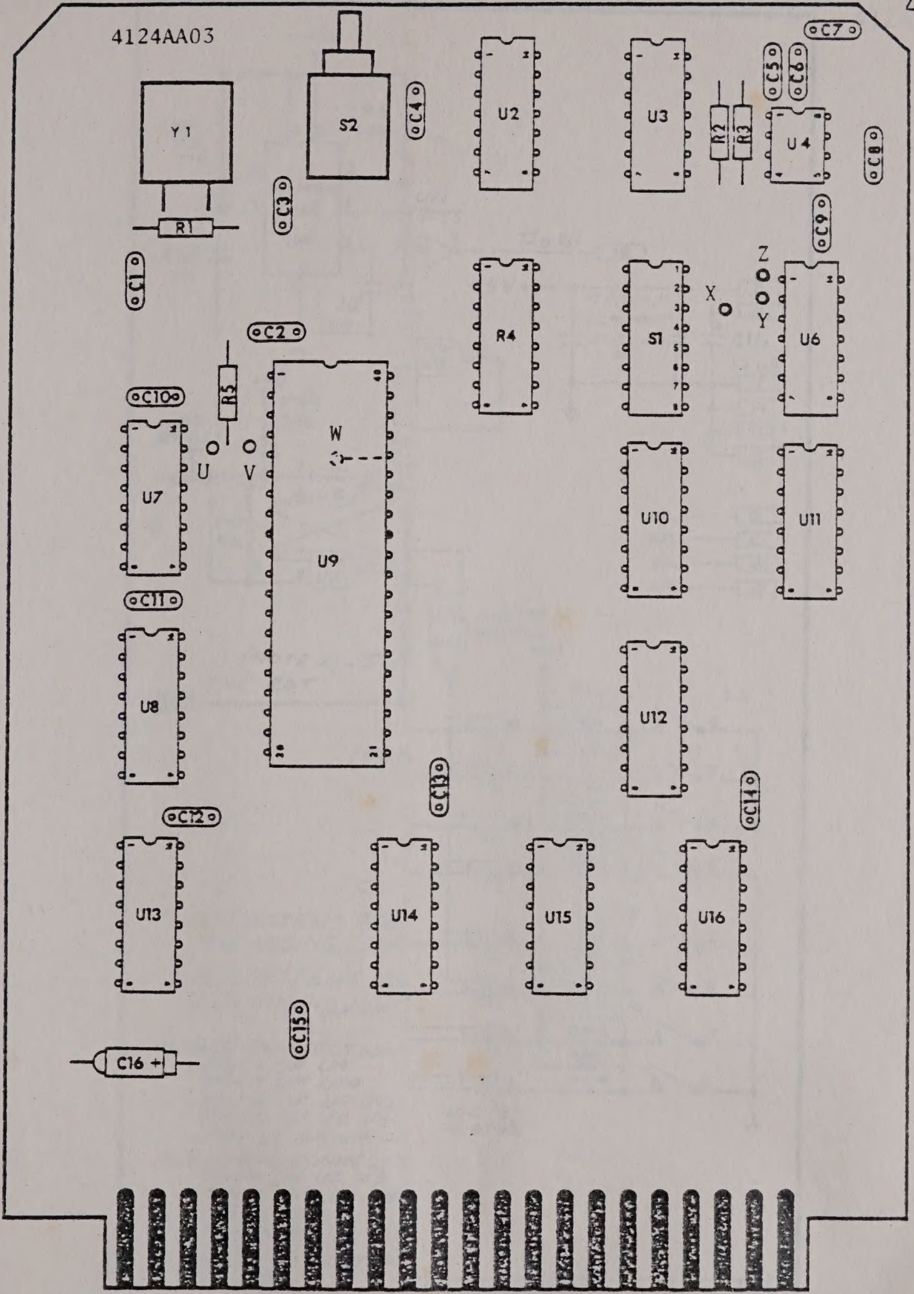
The System Controller parts are listed in the Bill of Material. A parts location drawing appears following the Bill of Material.


BINARY CODE SETTING
CMPTR U13
I/OEN
9
CNTL BUS
EQL
A11-A14
RESET
RECEIVER/ DRIVER U7, U8, U14-U16
R/W
16
ADRS BUS (A0-A15)
+5 VDC
RST
VMA
A15
2
TIMER U4
PON
RESET
μP U9
7
16
8
CNTL 7
ADRS 16
DATA 8
8
DATA BUS (D0-D7)
RST
4 MHz
2
2
BMVB U2
XTAL OSC Y1
TST
8
TEST SWITCH MATRIX S1-S8 U10, U12

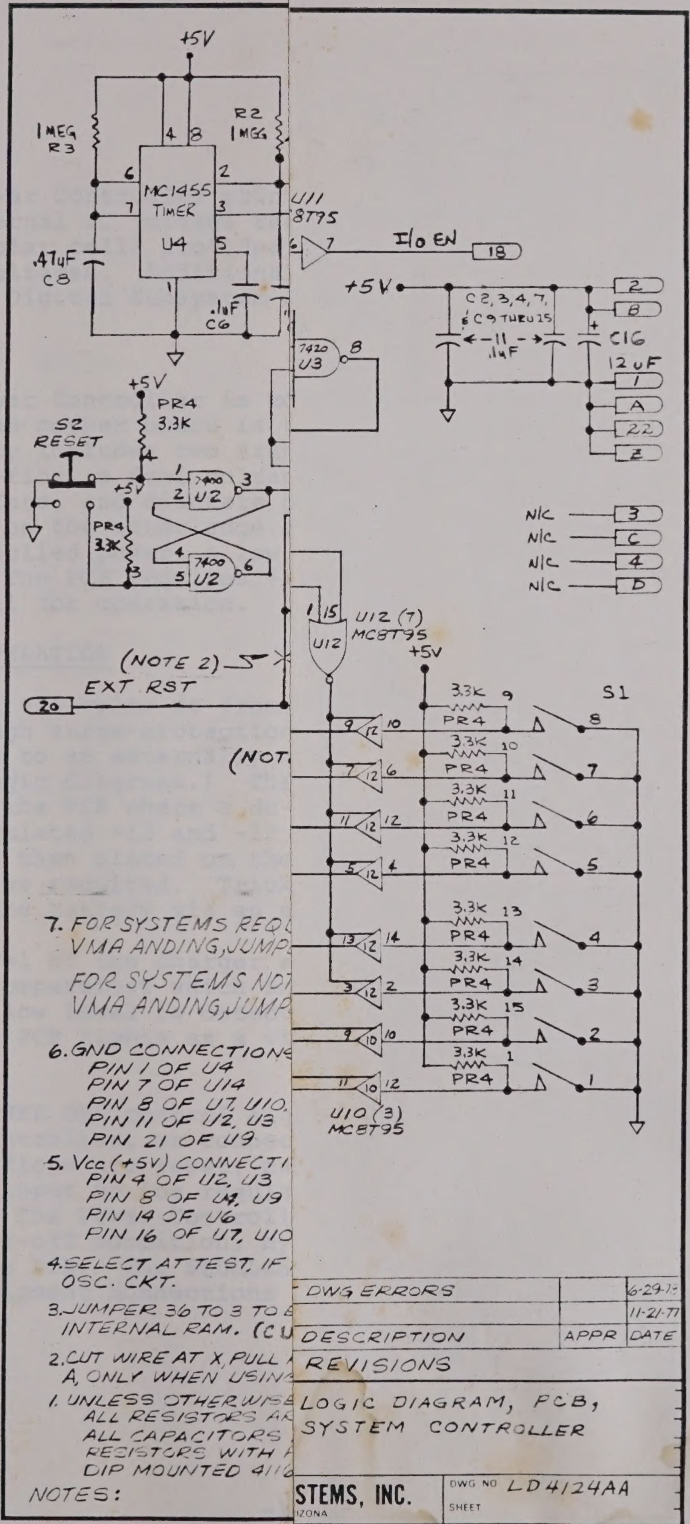
4124-1

System Controller PCB Block Diagram

BILL OF MATERIAL				NAME SYSTEM CONTROLLER PCB	NO. BM4124AA06
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4124AA03	ESI	BOARD, PRINTED CIRCUIT	
2	1	MC6802	MOTOROLA	I.C., MICROPROCESSOR	U9
3	1	MC1455	MOTOROLA	I.C., TIMING CIRCUIT	U4
4	1	74LS85	TI	I.C., 4 BIT COMPARATOR	U13
5	1	7400	TI	I.C., QUAD 2 INPUT NAND	U2
6	1	74LS08	TI	I.C., QUAD 2 INPUT NAND	U6
7	1	7420	TI	I.C., DUAL 4 INPUT NAND	U3
8	2	8216	INTEL	I.C., 4 BIT BI-DIR BUS DVR.	U15,U16
9	6	MC8T95	MOTOROLA	I.C., HEX TRI-STATE BUFFER	U7,8,10,11,12, 14
10	1	206-8	CTS	SWITCH, DIP, 8-SPST	S1
11	1	B8600	CUTLER HAMMER	SWITCH, SPDT, MOMENTARY	S2
12	1	MP04A	CTS	CRYSTAL, QUARTZ, 4MHz	Y1
13	1	ICN-406-S4G	ROBINSON NUGENT	SOCKET, 40 PIN, DIP (GOLD)	U9
14	1	RC07GF332J	COML	RESISTOR, 3.3K, ¼W, 5% CARBON	R5
15	1	RC07GF205J	COML	RESISTOR, 2 MEG, ¼W, 5% CARBON	R1
16	1	4116R-002-332	BOURNS	RESISTOR, DIP, 3.3K	PR4
17	2	RC07GF105J	COML	RESISTOR, 1 MEG, ¼W, 5% CARBON	R2,R3
18	1	196D126X9020JA1	SPRAGUE	CAPACITOR, TANTALUM, 12 uF, 20V, 20%	C16
19	1	CD6CD200J03	CORNING	CAPACITOR, 20pF, 500V, SIVLER MICA	C1
20	13	CY20C104M	CENTRALAB	CAPACITOR, 0.1uF, 50V CERAMIC DIP	C2 THRU C7, C9 THRU C15
21	1	CY20C474M	CENTRALAB	CAPACITOR, .47uF, 50V, CERAMIC DIP	C8


4124AA03
Y1
S2
C4
U2
U3
C7
C5
C6
R2
R3
U4
C8
C3
R1
C9
C1
R4
S1
X
Z
Y
U6
C2
C10
R5
W
U
V
U7
U9
U10
U11
C11
U8
U12
C13
C14
C12
U13
U14
U15
U16
C15
C16 +

System Controller PCB Parts Location


+5V
1MEG R3
R2 1MEG
MC1455 TIMER U4
4 8 6 7 2 3 5 1
U11 8T75
6 7
I/O EN
18
.47uF C8
.1uF C6
+5V
C2,3,4,7, & C9 THRU 15
← 11 →
.1uF
C16 12uF
2
B
1
A
22
Z
7420 U3
8
+5V
PR4 3.3K
S2 RESET
7400 U2
1 2 3 4 5 6
PR4 3.3K
N/C 3
N/C C
N/C 4
N/C D
U12 (7) MC8T95
1 15
U12
(NOTE 2)
X
EXT RST
20
(NOT
+5V
S1
3.3K PR4 9 10 11 12 13 14 15 1
8 7 6 5 4 3 2 1
9 12 10
7 12 6
11 12 12
5 12 4
13 12 14
3 12 2
9 10 10
11 10 12
U10 (3) MC8T95

7. FOR SYSTEMS REQ
VMA ANDING, JUMP
FOR SYSTEMS NOT
VMA ANDING, JUMP

6. GND CONNECTIONS
PIN 1 OF U4
PIN 7 OF U14
PIN 8 OF U7, U10,
PIN 11 OF U2, U3
PIN 21 OF U9

5. Vcc (+5V) CONNECTI
PIN 4 OF U2, U3
PIN 8 OF U4, U9
PIN 14 OF U6
PIN 16 OF U7, U10

4. SELECT AT TEST, IF
OSC. CKT.

3. JUMPER 36 TO 3 TO E
INTERNAL RAM. (C

2. CUT WIRE AT X, PULL
A, ONLY WHEN USIN

1. UNLESS OTHERWISE
ALL RESISTORS AR
ALL CAPACITORS
RESISTORS WITH P
DIP MOUNTED 411

NOTES:

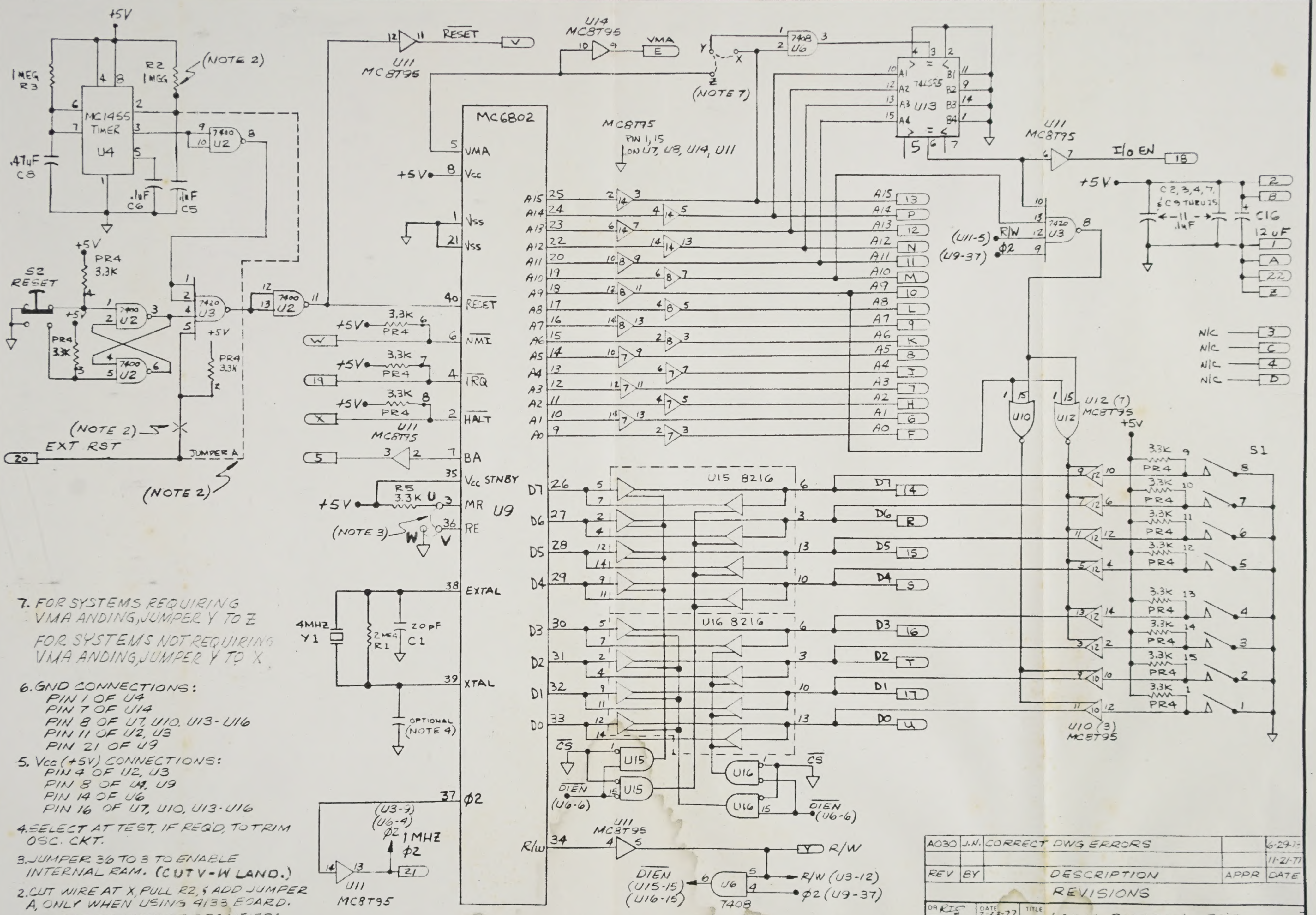
DESCRIPTION	APPR	DATE
DWG ERRORS		6-29-7
		11-21-77

REVISIONS

LOGIC DIAGRAM, PCB,
SYSTEM CONTROLLER

STEMS, INC.
IZONA

DWG NO LD4124AA
SHEET


+5V
1 MEG R3
R2 1 MEG
(NOTE 2)
MC1455 TIMER U4
.47uF C8
.1uF C6
.1uF C5
7400 U2
7420 U3
S2 RESET
PR4 3.3K
EXT RST
JUMPER A
(NOTE 2)
RESET
U11 MC8T95
U14 MC8T95
VMA
Y X Z
(NOTE 7)
7408 U6
74LS85 U13
MC6802
VMA
Vcc
Vss
RESET
NMI
IRQ
HALT
BA
Vcc STNBY
MR
RE
U9
EXTAL
XTAL
ϕ2
R/W
(NOTE 3)
4MHZ Y1
2 MEG R1
20pF C1
OPTIONAL (NOTE 4)
(U3-9) (U6-4) ϕ2
1 MHZ ϕ2
MC8T95
PIN 1, 15 ON U7, U8, U14, U11
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
U15 8216
U16 8216
CS
DIEN (U6-6)
I/O EN
(U11-5) R/W
(U9-37) ϕ2
7420 U3
C2, 3, 4, 7, & C9 THRU 15 .1uF
C16 12 uF
N/C
U10
U12 (7) MC8T95
U10 (3) MC8T95
S1
DIEN (U15-15) (U16-15)
U6 7408
R/W (U3-12)
ϕ2 (U9-37)
R/W

7. FOR SYSTEMS REQUIRING VMA ANDING, JUMPER Y TO Z

FOR SYSTEMS NOT REQUIRING VMA ANDING, JUMPER Y TO X

6. GND CONNECTIONS:
   PIN 1 OF U4
   PIN 7 OF U14
   PIN 8 OF U7, U10, U13-U16
   PIN 11 OF U2, U3
   PIN 21 OF U9

5. Vcc (+5V) CONNECTIONS:
   PIN 4 OF U2, U3
   PIN 8 OF U4, U9
   PIN 14 OF U6
   PIN 16 OF U7, U10, U13-U16

4. SELECT AT TEST, IF REQ'D, TO TRIM OSC. CKT.

3. JUMPER 36 TO 3 TO ENABLE INTERNAL RAM. (CUT V-W LAND.)

2. CUT WIRE AT X, PULL R2, & ADD JUMPER A, ONLY WHEN USING 4133 BOARD.

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5%, 1/4 W.
   ALL CAPACITORS ARE IN MICRO FARADS.
   RESISTORS WITH PIN # ARE BOURNS DIP MOUNTED 4116R-002-332.

NOTES:

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO ENGINEERED SYSTEMS, INC AND SHALL NOT BE USED FOR ENGINEERING, DESIGN, PROCUREMENT, OR MANUFACTURE IN WHOLE OR IN PART WITHOUT CONSENT OF ENGINEERED SYSTEMS, INC

REV	BY	DESCRIPTION	APPR	DATE
A030	J.N.	CORRECT DWG ERRORS		6-29-7
				11-21-77

REVISIONS

DR RJS DATE 2-23-77
APPR RNC DATE 5-17-77
ISSUE 04

TITLE LOGIC DIAGRAM, PCB, SYSTEM CONTROLLER

ENGINEERED SYSTEMS, INC.
PHOENIX, ARIZONA

DWG NO LD4124AA
SHEET

FUNCTION

The Power Controller printed circuit board (PCB) (together with an external IC voltage regulator, +12 Vdc battery, and power supply or solar cell) provides the system +5, +12, and -12 Vdc operating voltages. Additionally, the PCB provides an interrupt flag to the Digital Subsystem Controller if power fails.

DESCRIPTION

The Power Controller is mounted on a 4½ x 6½ inch PCB. Interface with the mother board is through a dual 22-pin edge connector. The circuitry includes two transorbers, three transistors, a dual D-type flip-flop, a dual voltage comparator, a dc-to-dc converter, two hex buffers, and discrete passive components. Three LED's are located on the outer edge of the PCB to provide visual indication of applied power, a low battery condition, and a low charger condition. The PCB requires +15 Vdc (nominal) from a power supply or solar cell for operation.

THEORY OF OPERATION

Nominal +15 volts dc from the dc supply or solar cell is passed through surge-protection, voltage conversion, and switching circuits to an externally mounted IC voltage regulator. (See block and logic diagrams.) The regulator returns regulated +5 volts dc to the PCB where a dc-to-dc converter converts the +5 volts to regulated +12 and -12 volts dc. These three operating voltages are then placed on the system voltage bus for use by other PCB's as required. Trickle charge current is sent from the charger to the battery via an external diode circuit.

The level of the charger and power supply voltages are sensed by voltage comparators which initiate interrupt flags (CHGR and LOBAT) if a low level is detected. Simultaneously, a LED indicator on the PCB lights as a visual alarm of the low level condition.

If a POWER OFF control signal is received from the Digital Subsystem Controller, or connector J8 on the mother board, the two D-type flip-flops are reset, causing the control switch to disconnect the input to the regulator and an interrupt flag (TXFLAG) to be sent. The Power Controller is returned to operating condition after a power-off condition, by pressing the mementary-close toggle switch on the PCB. The SQUELCH and EXT XMT lines are used for external equipment connections (J8 on mother board) in some system applications.

ADJUSTMENTS

The Power Controller PCB contains one adjustment, LOBAT level adjustment R6. (See logic diagram and parts location drawing.)

LOBAT LEVEL. Set the low battery threshold level with the test equipment listed below, or equivalent, using the procedural steps that follow:

Extender Board	ESI 4131
Rheostat	Commercial
Digital VOM	H-P 3439A

1. Install PCB on extender board in mother board.

2. Connect rheostat between battery positive output terminal and +12 Vdc (+BAT) input to PCB.

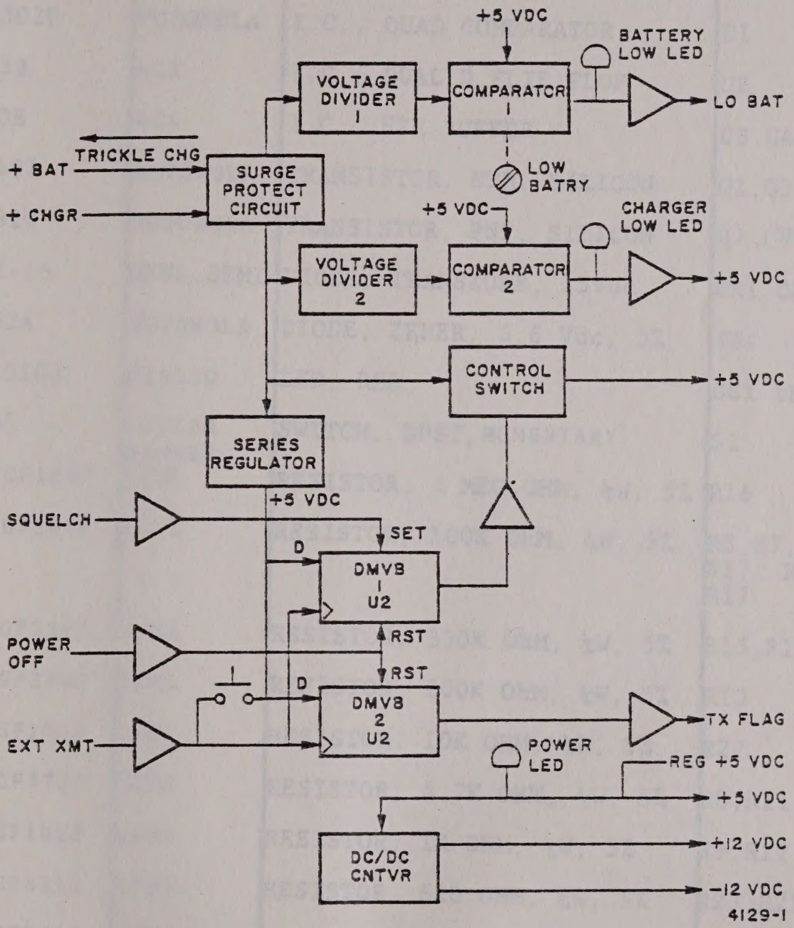
3. Connect digital VOM between rheostat output and system voltage return bus.

4. Set rheostat for +11.8 volt reading on meter.

5. Adjust LOBAT level potentiometer R6 until the BATTERY LOW LED indicator on the PCB just lights.

PARTS LIST

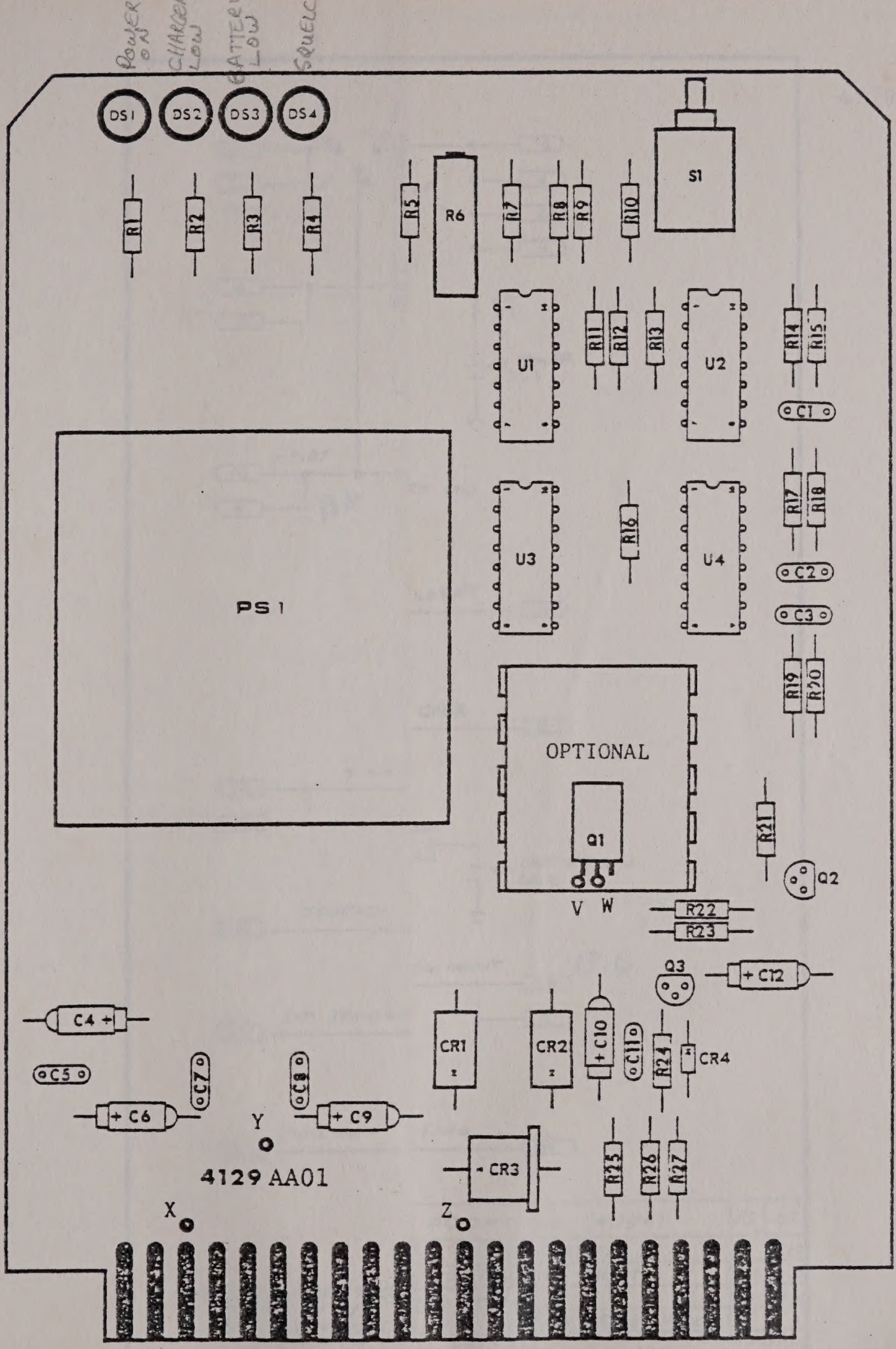
The Power Controller parts are listed in the Bill of Material. A parts location drawing appears following the Bill of Material.


+5 VDC
BATTERY LOW LED
VOLTAGE DIVIDER 1
COMPARATOR 1
LO BAT
TRICKLE CHG
+ BAT
+ CHGR
SURGE PROTECT CIRCUIT
LOW BATRY
+5 VDC
CHARGER LOW LED
VOLTAGE DIVIDER 2
COMPARATOR 2
+5 VDC
CONTROL SWITCH
+5 VDC
SERIES REGULATOR
+5 VDC
SQUELCH
SET
D
DMVB 1 U2
POWER OFF
RST
RST
D
DMVB 2 U2
TX FLAG
EXT XMT
POWER LED
REG +5 VDC
+5 VDC
+12 VDC
DC/DC CNTVR
-12 VDC
4129-1

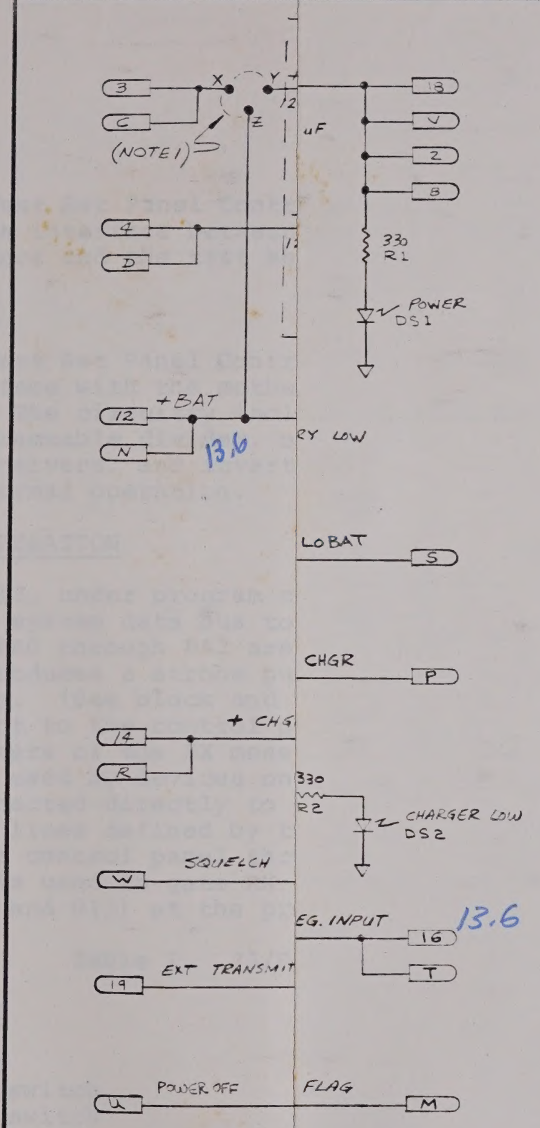
Power Controller PCB Block Diagram

BILL OF MATERIAL				NAME POWER CONTROLLER PCB	NO. BM4129AA03
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4129AA01	ESI	BOARD, PRINTED WIRING	
2	1	MC3302P	MOTOROLA	I.C., QUAD COMPARATOR	U1
3	1	4013B	RCA	I.C., DUAL D FLIP FLOP	U2
4	2	4050B	RCA	I.C., HEX BUFFER	U3,U4
5	2	2N4401	MOTOROLA	TRANSISTOR, NPN, SILICON	Q2,Q3
6	1	2N4920	MOTOROLA	TRANSISTOR, PNP, SILICON	Q1 (OPTIONAL)
7	2	ICTE-15	GENL.SEMI	DIODE, TRANSZORB, 15Vdc.	CR1,CR2
8	1	1N752A	MOTOROLA	DIODE, ZENER, 5.6 Vdc, 5%	CR4
9	4	550-0103	DIALCO	LED, RED	DS1 thru DS4
10	1	88600	CUTLER HAMMER	SWITCH, DPST, MOMENTARY	S1
11	1	RC07GF105J	COML	RESISTOR, 1 MEG OHM, ¼W, 5%	R16
12	9	RC07GF104J	COML	RESISTOR, 100K OHM, ¼W, 5%	R5,R7,R13,R14, R17, R19,R25,R26 R17
13	3	RC07GF334J	COML	RESISTOR, 330K OHM, ¼W, 5%	R15,R18,R20
14	1	RC07GF204J	COML	RESISTOR, 200K OHM, ¼W, 5%	R10
15	1	RC07GF103J	COML	RESISTOR, 10K OHM, ¼W, 5%	R22
16	2	RC07GF472J	COML	RESISTOR, 4.7K OHM, ¼W, 5%	R8,R11
17	3	RC07GF102J	COML	RESISTOR, 1K OHM, ¼W, 5%	R9,R12,R24
18	2	RC07GF621J	COML	RESISTOR, 620 OHM, ¼W, 5%	R23,R21
19	4	RC07GF331J	COML	RESISTOR, 330 OHM, ¼W, 5%	R3,R4,R1,R2
20	1	3009	BOURNS	POTENTIONMETER, 100K OHM	R6
21	5	196D126X9020 JA1	SPRAGUE	CAPACITOR, TANTALUM, 12uF, 20V,20%	C4,6,9,10,12
22	1	THM6101-13	THERMALOY	HEATSINK	
23	3	CY15C103M	CENTRALAB	CAPACITOR, .01 uF, 50VDC, CERAMIC DIP	C1,2,3
24	4	CY20C104M	CENTRALAB	CAPACITOR, .1 uF, 50VDC, CERAMIC DIP	C5,7,8,11

BILL OF MATERIAL		NAME POWER CONTROLLER PCB			NO. BM4129AA03
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
25	1	546	BURR-BROW	CONVERTER, DC TO DC	PS1


POWER ON
CHARGE LOW
BATTER LOW
SQUELC
DS1
DS2
DS3
DS4
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
S1
U1
U2
U3
U4
R11
R12
R13
R14
R15
C1
R16
R17
R18
C2
C3
R19
R20
PS1
OPTIONAL
Q1
V
W
R21
Q2
R22
R23
Q3
+ C12
C4 +
C5
+ C6
C7
C8
+ C9
CR1
CR2
+ C10
C11
R24
CR4
Y
CR3
R25
R26
R27
4129 AA01
X
Z

Power Controller PCB Parts Location


3
C
X
Y
Z
(NOTE 1)
12
uF
13
V
2
B
4
D
12
330
R1
POWER
DS1
+BAT
12
N
13.6
RY LOW
LOBAT
S
CHGR
P
+ CHG
14
R
330
R2
CHARGER LOW
DS2
SQUELCH
W
EG. INPUT
16
T
13.6
EXT TRANSMIT
19
POWER OFF
FLAG
U
M

4. GND CONNECTION
PIN 7 OF U2
PIN 8 OF U3, U4
PIN 12 OF U1

3. Vcc (+5V) CONNEC
PIN 1 OF U3

2. REMOVE Q1 AND
FOR CONTINUOUS

1. JUMPER X TO Y FO
JUMPER X TO Z FO

NOTES:

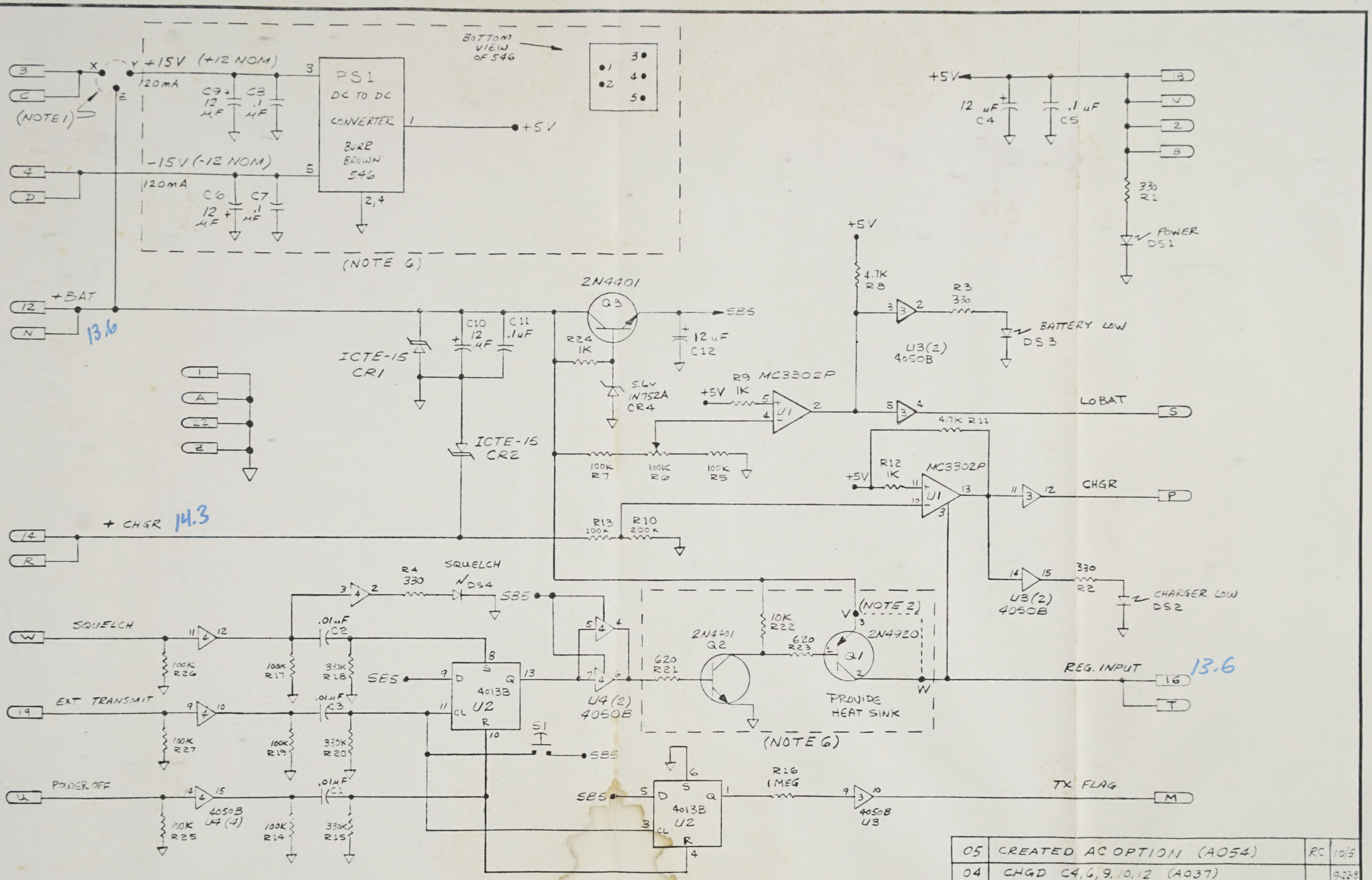
AC OPTION (A054)	RC	10/5
,6,9,10,12 (A037)		9-22-8
DWG ERRORS (A037)	J.N.	7-5-7
OTE TWO	DLF	5/02/78
D1 - 1N4719 ,ADDED NOTE 1		
RELEASE	RB	5/17/7
SCRIPTION	BY	DATE

VISIONS

LOGIC DIAGRAM, PCB,
POWER CONTROLLER

YSTEMS, INC.
RIZONA

DWG NO LD4129AA
SHEET SHT 1 OF 1


BOTTOM VIEW OF 546
+15V (+12 NOM)
120mA
-15V (-12 NOM)
120mA
(NOTE 1)
PS1
DC TO DC CONVERTER
BURR BROWN 546
+5V
(NOTE 6)
C9 12 µF
C8 .1 µF
C6 12 µF
C7 .1 µF
+BAT
13.6
2N4401
Q3
SB5
12 uF C12
C10 12 µF
C11 .1uF
ICTE-15 CR1
ICTE-15 CR2
R24 1K
5.6V 1N752A CR4
+5V
4.7K R8
R9 1K
MC3302P
U1
U3(2) 4050B
R3 330
BATTERY LOW DS3
LOBAT
4.7K R11
R12 1K
MC3302P
CHGR
100K R7
100K R6
100K R5
+ CHGR
14.3
R13 100K
R10 200K
12 uF C4
.1 uF C5
330 R1
POWER DS1
U3(2) 4050B
330 R2
CHARGER LOW DS2
(NOTE 2)
10K R22
620 R23
2N4920
Q1
2N4401
Q2
620 R21
PROVIDE HEAT SINK
(NOTE 6)
REG. INPUT
13.6
R4 330
SQUELCH DS4
SQUELCH
.01uF C2
100K R26
100K R17
330K R18
SES
4013B U2
U4(2) 4050B
EXT TRANSMIT
.01uF C3
100K R27
100K R19
330K R20
S1
POWER OFF
4050B U4(4)
.01uF C1
100K R25
100K R14
330K R15
4013B U2
R16 1MEG
4050B U3
TX FLAG
3
C
4
D
12
N
1
A
22
Z
14
R
W
19
U
13
V
2
B
S
P
16
T
M

4.GND CONNECTIONS:
PIN 7 OF U2
PIN 8 OF U3, U4
PIN 12 OF U1

3.Vcc (+5V) CONNECTIONS:
PIN 1 OF U3

2. REMOVE Q1 AND JUMPER V TO W
FOR CONTINUOUS MODE OPERATION.

1. JUMPER X TO Y FOR LOADS ≦ 100 mA;
JUMPER X TO Z FOR LOADS < 100 mA.

NOTES:

6. PARTS NOT USED ON 4129AC
OPTION. JUMPER X TO Z
AND V TO W.

5. SB5 (+5V) CONNECTIONS:
PIN 1 OF U4
PIN 14 OF U2

05	CREATED AC OPTION (A054)	RC	10/5
04	CHGD C4, 6, 9, 10, 12 (A037)		9-22-8
03	CORRECT DWG ERRORS (A037)	J.N.	7-5-7
02	ADDED NOTE TWO	DLF	5/02/7
01	REMOVED D1 - 1N4719, ADDED NOTE 1		
—	INITIAL RELEASE	RB	5/17/7
REV	DESCRIPTION	BY	DATE

REVISIONS

DR KS DATE 4-18-77
APPR RMS DATE 5-17-77
ISSUE 05
TITLE LOGIC DIAGRAM, PCB, POWER CONTROLLER

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ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA
DWG NO LD4129AA
SHEET SHT 1 OF 1

FUNCTION

The Test Set Panel Controller printed circuit board (PCB) provides the interface between the test set front panel controls and indicators and the test set microprocessor logic.

DESCRIPTION

The Test Set Panel Controller is mounted on a 4½ x 6½ inch PCB. Interface with the mother board is through a 22-pin edge connector. The circuitry includes a peripheral interface adapter (PIA), programmable divider, octal decoder, D-type flip-flops, drivers, receivers, and inverters. The PCB requires +5 and +12 volts for normal operation.

THEORY OF OPERATION

PIA U12, under program control, transfers the 8-bit digital data on the system data bus to two 8-bit I/O busses (PA0-PA7 and PB0-PB7). PA0 through PA2 are used as the inputs to octal decoder U13 which produces a strobe pulse (STR1-STR7) as a function of the octal coding. (See block and logic diagrams.) Strobes STR5 and STR6 are sent to the control panel to enable the LSD and MSD display characters of the RX message display indicator. The other six strobes are used by devices on the PCB as timing pulses. PA3 through PA5 are connected directly to the control panel to provide the input command lines defined by table I. PA6, an output signal, connects to the control panel through a driver (U7-13) at the STR2 time. PA7 is used to gate RX frame select switch data through receivers (U9 and U11) at the programmed time.

Table I. J3/PIA Signals

PANEL DEVICE	PIA PORT	PIA I/O
ENTER switch	CB1	In
TX INITIATE switch	CB2	In
AUTO/MANUAL switch	PA3	In
Central/Remote mode (PERSONALITY PROG)	PA4	In
AUX/HEX switch	PA5	In
MSG VALID indicator	PA6	Out

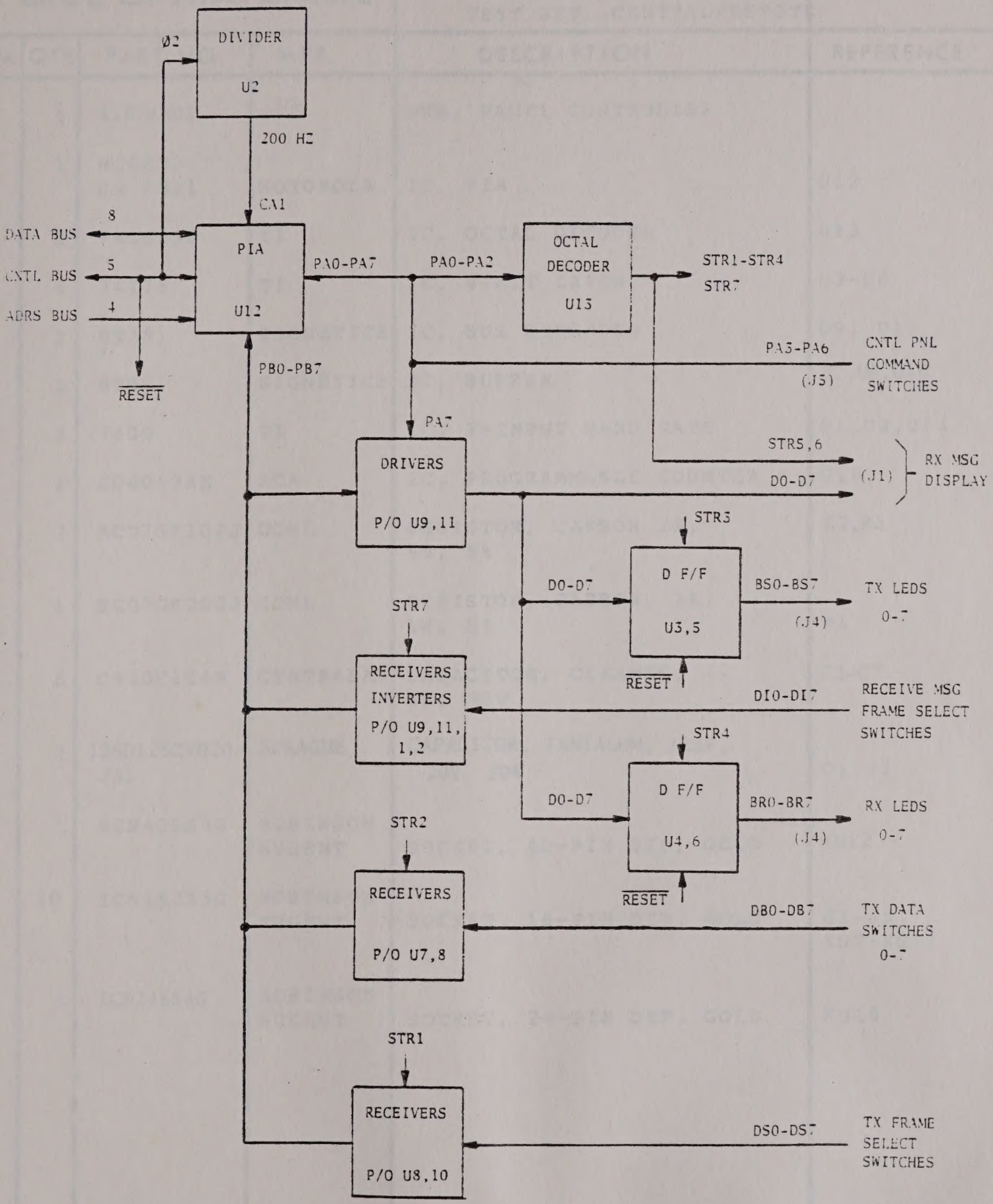
The other PIA 8-bit data bus (PB0-PB7) carries input/output data to/from the control panel and the PIA registers at times governed by the strobe pulses. The PB0-PB7 signals that drive the TX and RX data LED's are passed through drivers (U9 and U11) to the D inputs of flip-flops U3 - U6 when PA7 is high. Then the positive edge of STR3 clocks these data to the Q outputs (BS0-BS7) and

through J4 to the TX data LED's. Similarly, when STR4 rises, the BR0-BR7 signals are applied to the RX data LED's. The system RESET control signal is used to clear the flip-flops after each transition.

Switch position information from the FRAME SELECT (TX) thumbwheel switches, the eight TX data switches, and the RECEIVE MSG (RX frame select) thumbwheel switches are strobed through receivers at times STR1, STR2, and STR7, respectively, on the PB0-PB7 lines into the PIA registers and subsequently transferred to the system data bus.

PARTS LIST

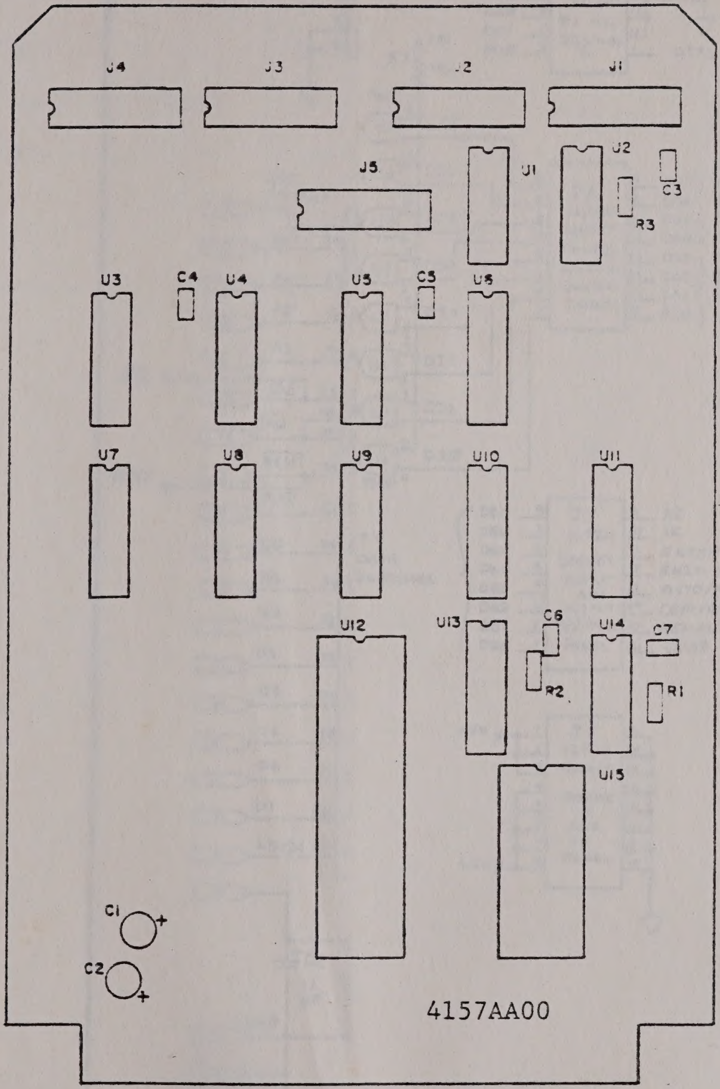
The Test Set Panel Controller parts are listed in the Bill of Material. A parts location drawing appears following the Bill of Material.


DIVIDER
U2
Ø2
200 HZ
CA1
8
DATA BUS
5
CNTL BUS
4
ADRS BUS
RESET
PIA
U12
PA0-PA7
PA0-PA2
OCTAL DECODER
U13
STR1-STR4
STR7
PA3-PA6
(J5)
CNTL PNL COMMAND SWITCHES
PB0-PB7
PA7
DRIVERS
P/O U9,11
STR5,6
D0-D7
(J1)
RX MSG DISPLAY
STR3
D F/F
U3,5
D0-D7
BS0-BS7
(J4)
TX LEDS 0-7
RESET
STR7
RECEIVERS INVERTERS
P/O U9,11, 1,2
DI0-DI7
RECEIVE MSG FRAME SELECT SWITCHES
STR4
D F/F
U4,6
D0-D7
BR0-BR7
(J4)
RX LEDS 0-7
RESET
STR2
RECEIVERS
P/O U7,8
DB0-DB7
TX DATA SWITCHES 0-7
STR1
RECEIVERS
P/O U8,10
DS0-DS7
TX FRAME SELECT SWITCHES

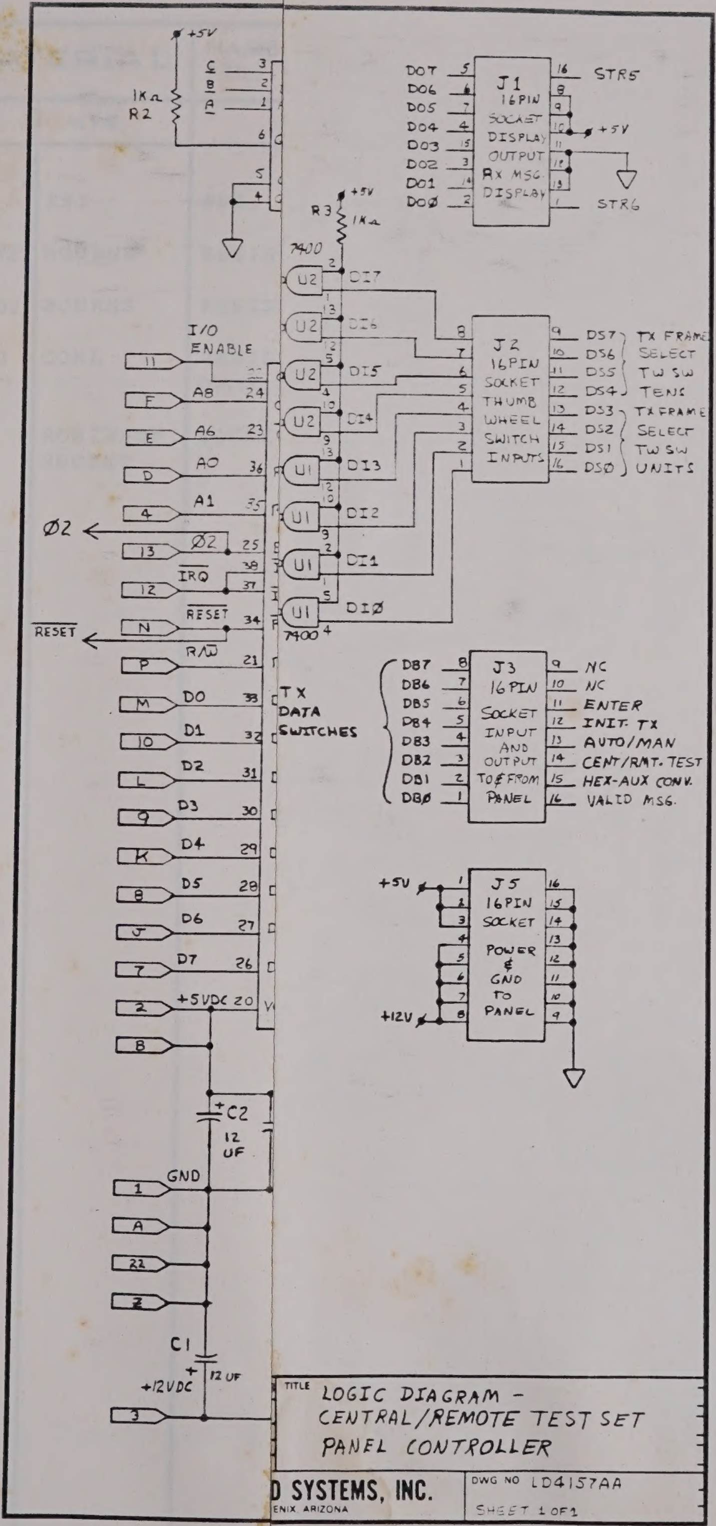
Test Set Panel Controller PCB Block Diagram

BILL OF MATERIAL	NAME PANEL CONTROLLER, TEST SET, CENTRAL/REMOT	NO. BM4157AA01

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4157AA01	ESI	PWB, PANEL CONTROLLER	
2	1	MC6820 OR 6821	MOTOROLA	IC, PIA	U12
3	1	74LS138	TI	IC, OCTAL DECODER	U13
4	4	74175	TI	IC, 4-BIT LATCH	U3-U6
5	2	8T28	SIGNETICS	IC, BUS EXTENDER	U9, U11
6	3	8T98	SIGNETICS	IC, BUFFER	U7,U8,U10
7	3	7400	TI	IC, 2-INPUT NAND GATE	U1,U2,U14
8	1	CD4059AE	RCA	IC, PROGRAMMABLE COUNTER	U15
9	2	RC07GF102J	COML	RESISTOR, CARBON 1K, ¼W, 5%	R2,R3
10	1	RC07GF202J	COML	RESISTOR, CARBON, 2K, ¼W, 5%	R1
11	5	CY20C104M	CENTRALAB	CAPACITOR, CERAMIC, .1 uF, 50V	C3-C7
12	2	196D126X9020-JA1	SPRAGUE	CAPACITOR, TANTALUM, 12uF, 20V, 20%	C1,C2
13	1	ICN406S4G	ROBINSON NUGENT	SOCKET, 40-PIN DIP, GOLD	XU12
14	10	ICN163S3G	ROBINSON NUGENT	SOCKET, 16-PIN DIP, GOLD	J1-J5, XU7-XU11
15	1	ICN246S4G	ROBINSON NUGENT	SOCKET, 24-PIN DIP, GOLD	XU15


J4
J3
J2
J1
J5
U1
U2
C3
R3
U3
C4
U4
U5
C5
U6
U7
U8
U9
U10
U11
U12
U13
C6
U14
C7
R2
R1
U15
C1
C2
+
+
4157AA00

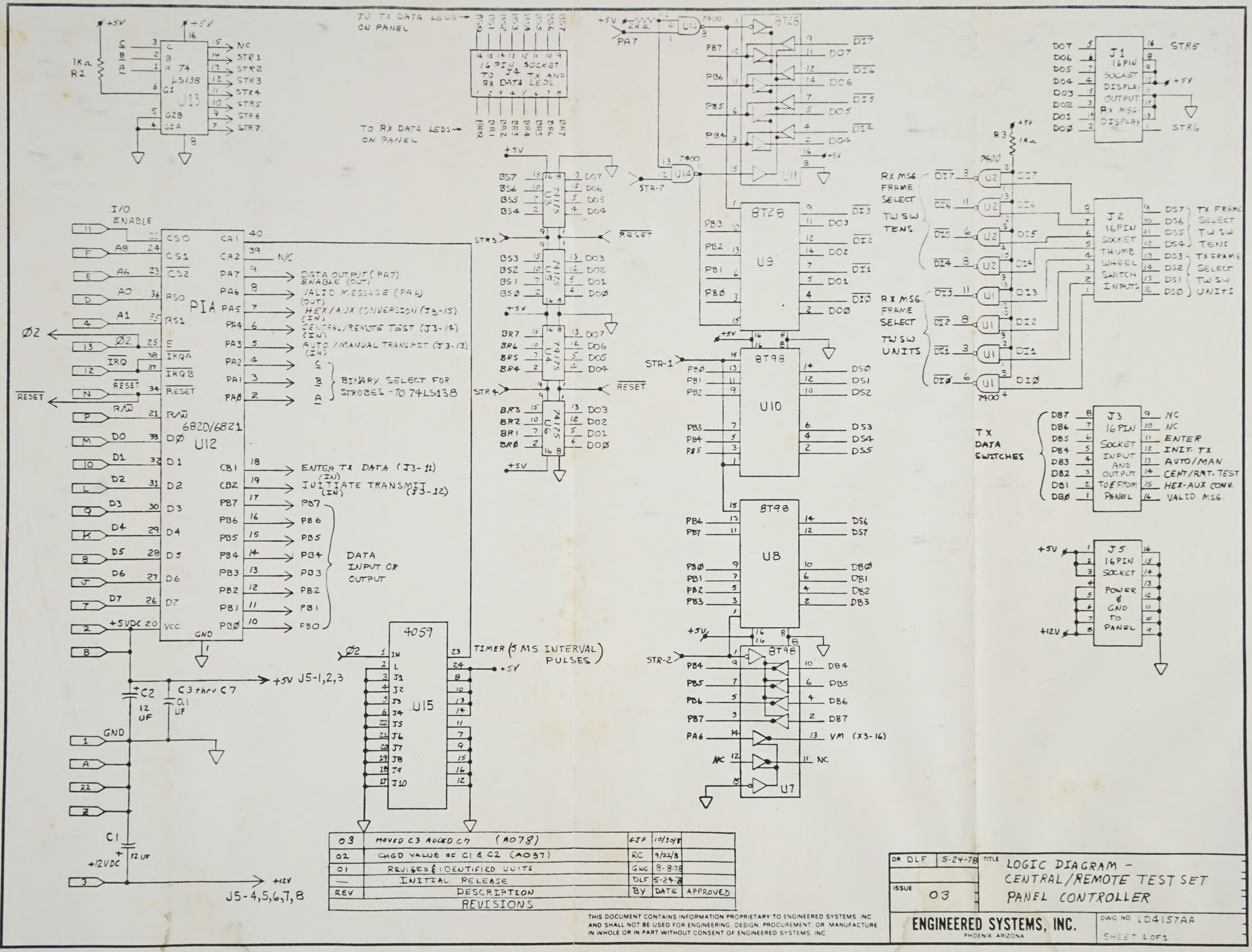
Test Set Panel Controller PCB Parts Location


+5V
1KΩ
R2
C
B
A
3
2
1
6
5
4
R3
1KΩ
7400
U2
U1
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DIØ
I/O ENABLE
11
F
E
D
4
13
12
N
P
M
10
L
9
K
8
J
7
2
B
1
A
22
Z
3
A8
A6
A0
A1
Ø2
IRQ
RESET
R/W
D0
D1
D2
D3
D4
D5
D6
D7
+5VDC
GND
+12VDC
C1
12 UF
C2
12 UF
TX DATA SWITCHES
D0T
D06
D05
D04
D03
D02
D01
D0Ø
J1
16PIN
SOCKET
DISPLAY
OUTPUT
RX MSG.
DISPLAY
STR5
STR6
J2
16PIN
SOCKET
THUMB
WHEEL
SWITCH
INPUTS
DS7
DS6
DS5
DS4
DS3
DS2
DS1
DSØ
TX FRAME SELECT TW SW TENS
TX FRAME SELECT TW SW UNITS
J3
16PIN
SOCKET
INPUT AND OUTPUT
TO & FROM PANEL
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
NC
NC
ENTER
INIT. TX
AUTO/MAN
CENT/RMT. TEST
HEX-AUX CONV.
VALID MSG.
J5
16PIN
SOCKET
POWER & GND TO PANEL
+5V
+12V

TITLE LOGIC DIAGRAM -
CENTRAL/REMOTE TEST SET
PANEL CONTROLLER

D SYSTEMS, INC.
ENIX, ARIZONA

DWG NO LD4157AA
SHEET 1 OF 1


74LS138
U13
1KΩ R2
STR1
STR2
STR3
STR4
STR5
STR6
STR7
TO TX DATA LEDS ON PANEL
16 PIN SOCKET TO J4 TX AND RX DATA LEDS
TO RX DATA LEDS ON PANEL
I/O ENABLE
PIA
6820/6821
U12
DATA OUTPUT (PA7) ENABLE (OUT)
VALID MESSAGE (PA6) (OUT)
HEX/AUX CONVERSION (J3-15) (IN)
CENTRAL/REMOTE TEST (J3-14) (IN)
AUTO/MANUAL TRANSMIT (J3-13) (IN)
BINARY SELECT FOR STROBES - TO 74LS138
ENTER TX DATA (J3-11) (IN)
INITIATE TRANSMIT (J3-12) (IN)
DATA INPUT OR OUTPUT
74175
U3
U5
U4
U6
RESET
Ø2
4059
U15
TIMER (5 MS INTERVAL PULSES)
+5V J5-1,2,3
C2 12 UF
C3 thru C7 0.1 UF
GND
C1 12 UF
+12VDC
+12V
J5-4,5,6,7,8
7400
U14
8T28
U11
U9
8T98
U10
U8
U7
STR-7
STR-1
STR-2
VM (X3-16)
NC
R3 1KΩ
U2
U1
RX MSG FRAME SELECT TW SW TENS
RX MSG FRAME SELECT TW SW UNITS
J1 16 PIN SOCKET DISPLAY OUTPUT RX MSG DISPLAY
J2 16 PIN SOCKET THUMB WHEEL SWITCH INPUTS
TX FRAME SELECT TW SW TENS
TX FRAME SELECT TW SW UNITS
TX DATA SWITCHES
J3 16 PIN SOCKET INPUT AND OUTPUT TO/FROM PANEL
ENTER
INIT. TX
AUTO/MAN
CENT/RMT. TEST
HEX-AUX CONV.
VALID MSG.
J5 16 PIN SOCKET POWER & GND TO PANEL

REV	DESCRIPTION	BY	DATE	APPROVED
03	MOVED C3 ADDED C7 (A078)	GJF	10/30/8	
02	CHGD VALUE OF C1 & C2 (A037)	RC	9/22/8	
01	REVISED & IDENTIFIED UNITS	GWG	8-8-78	
—	INITIAL RELEASE	DLF	5-24-78	

REVISIONS

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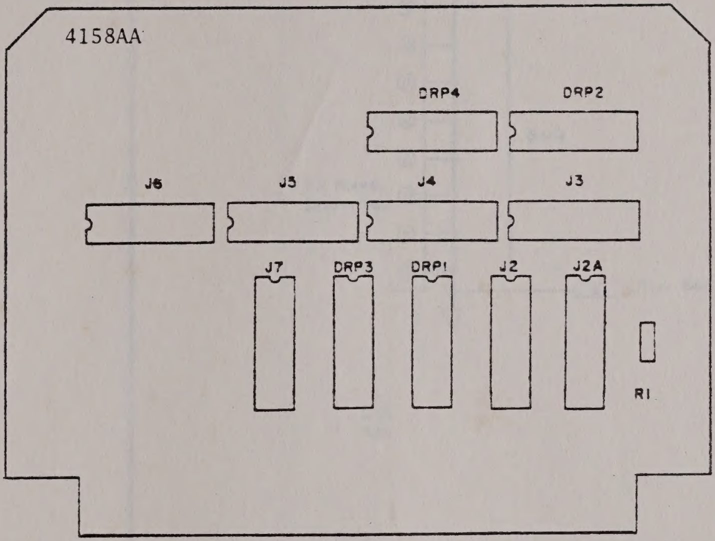
DR DLF 5-24-78
TITLE LOGIC DIAGRAM - CENTRAL/REMOTE TEST SET PANEL CONTROLLER
ISSUE 03
ENGINEERED SYSTEMS, INC.
PHOENIX, ARIZONA
DWG NO LD4157AA
SHEET 1 OF 1

BILL OF MATERIAL

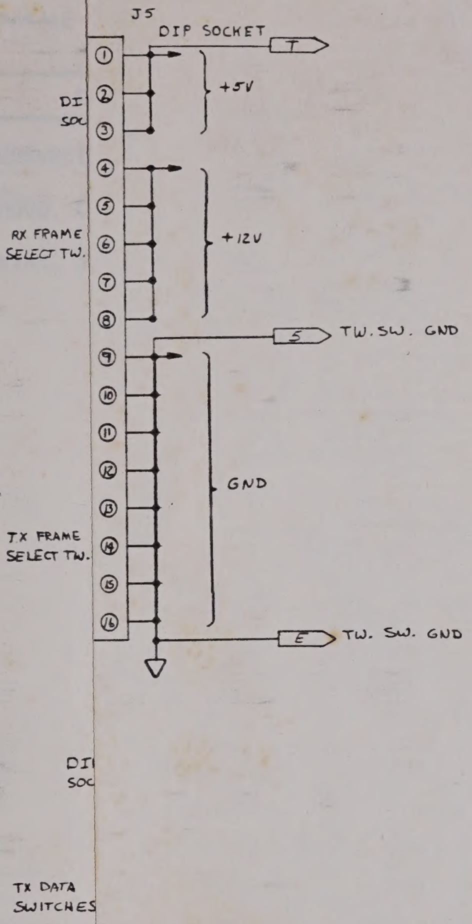
NAME PANEL INTERCONNECTION PCB, CENTRAL/REMOTE TEST SET

NO. BM4158AA01

ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	4158AA02	ESI	PWB, PANEL INTERCONNECTION	
2	2	4116R002-332	BOURNS	RESISTOR, DIP MOUNTED	PR1, PR2
3	2	4116R001-331	BOURNS	RESISTORS, DIP MOUNTED	PR3, PR4
4	1	RC07GF331J	COML	RESISTOR, CARBON, 330 OHMS, ¼W, 5%	R1
5	7	ICN163S3G	ROBINSON NUGENT	SOCKET, 16-PIN DIP	J2,J2A,J3-J7


4158AA
DRP4
DRP2
J6
J5
J4
J3
J7
DRP3
DRP1
J2
J2A
R1

Panel Interconnection PCB Parts Location


J5
DIP SOCKET
T
1
2
3
+5V
4
5
6
7
8
+12V
5
TW. SW. GND
9
10
11
12
13
14
15
16
GND
E
TW. SW. GND
DI
SOC
RX FRAME
SELECT TW.
TX FRAME
SELECT TW.
DI
SOC
TX DATA
SWITCHES

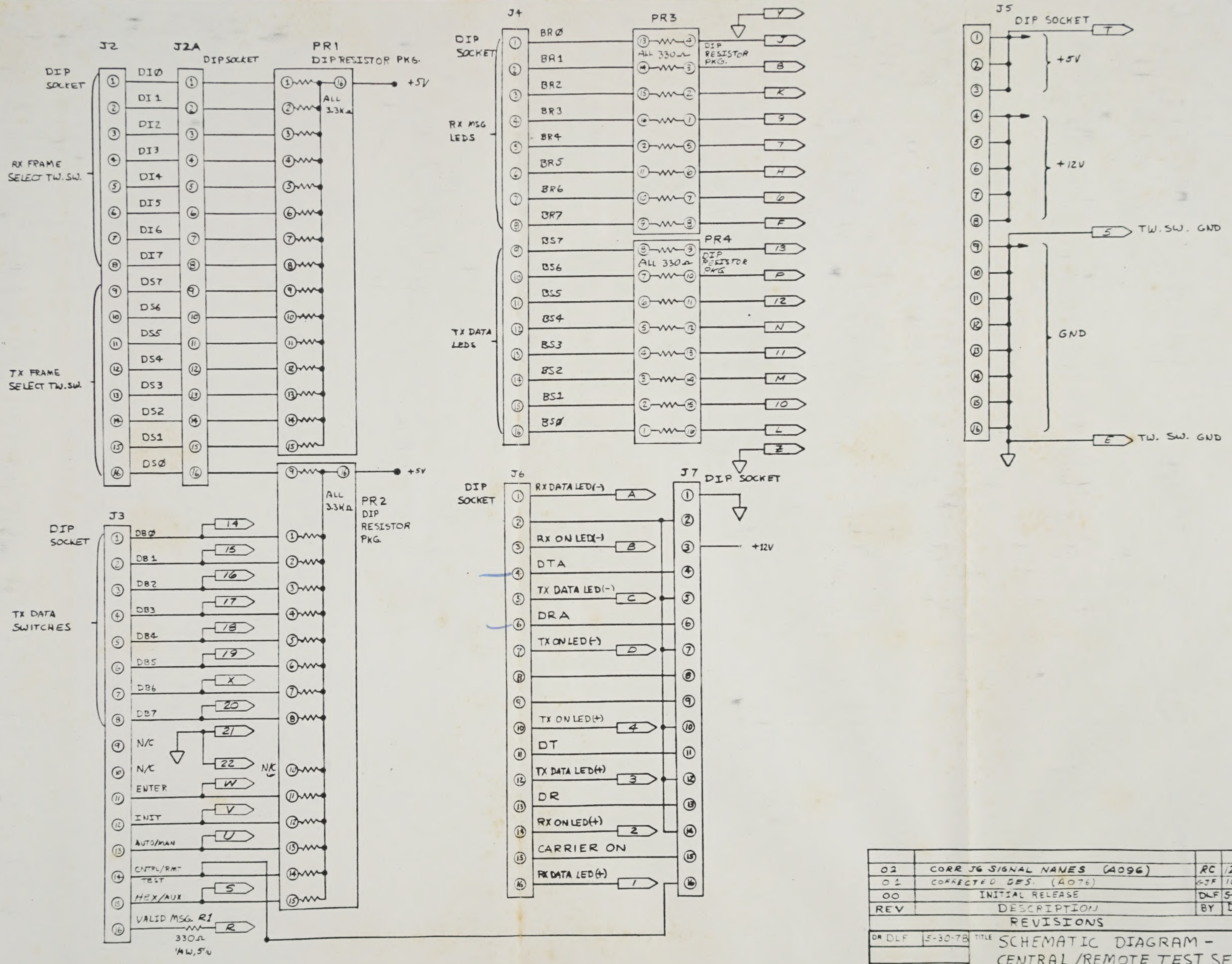
J6 SIGNAL NAMES (A096)	RC	12/20/8
TED DES. (A076)	GJF	10-31-8
INITIAL RELEASE	DLF	5-30-78
DESCRIPTION	BY	DATE

REVISIONS

TITLE SCHEMATIC DIAGRAM -
CENTRAL /REMOTE TEST SET
PANEL INTERCONNECTION BOARD

) SYSTEMS, INC.
ENIX ARIZONA

DWG NO
SD4158AA


J2
J2A
DIP SOCKET
PR1
DIP RESISTOR PKG.
+5V
ALL 3.3KΩ
DIP SOCKET
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DS7
DS6
DS5
DS4
DS3
DS2
DS1
DS0
RX FRAME SELECT TW. SW.
TX FRAME SELECT TW. SW.
+5V
ALL 3.3KΩ
PR2 DIP RESISTOR PKG
J3
DIP SOCKET
TX DATA SWITCHES
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
N/C
N/C
ENTER
INIT
AUTO/MAN
CNTRL/RMT TEST
HEX/AUX
VALID MSG. R1
330Ω ¼W, 5%
14
15
16
17
18
19
X
20
21
22
N/C
W
V
U
S
R
J4
DIP SOCKET
RX MSG LEDS
TX DATA LEDS
BR0
BR1
BR2
BR3
BR4
BR5
BR6
BR7
BS7
BS6
BS5
BS4
BS3
BS2
BS1
BS0
PR3
ALL 330Ω
DIP RESISTOR PKG.
PR4
ALL 330Ω
DIP RESISTOR PKG
Y
J
B
K
9
7
H
6
F
13
P
12
N
11
M
10
L
Z
J5
DIP SOCKET
T
+5V
+12V
S
TW. SW. GND
GND
E
TW. SW. GND
J6
DIP SOCKET
RX DATA LED(-)
RX ON LED(-)
DTA
TX DATA LED(-)
DRA
TX ON LED(-)
TX ON LED(+)
DT
TX DATA LED(+)
DR
RX ON LED(+)
CARRIER ON
RX DATA LED(+)
A
B
C
D
4
3
2
1
J7
DIP SOCKET
+12V

REV	DESCRIPTION	BY	DATE
02	CORR J6 SIGNAL NAMES (A096)	RC	12/20/8
01	CORRECTED DES. (A076)	GJF	10-31-8
00	INITIAL RELEASE	DLF	5-30-78

REVISIONS

DR DLF 5-30-78

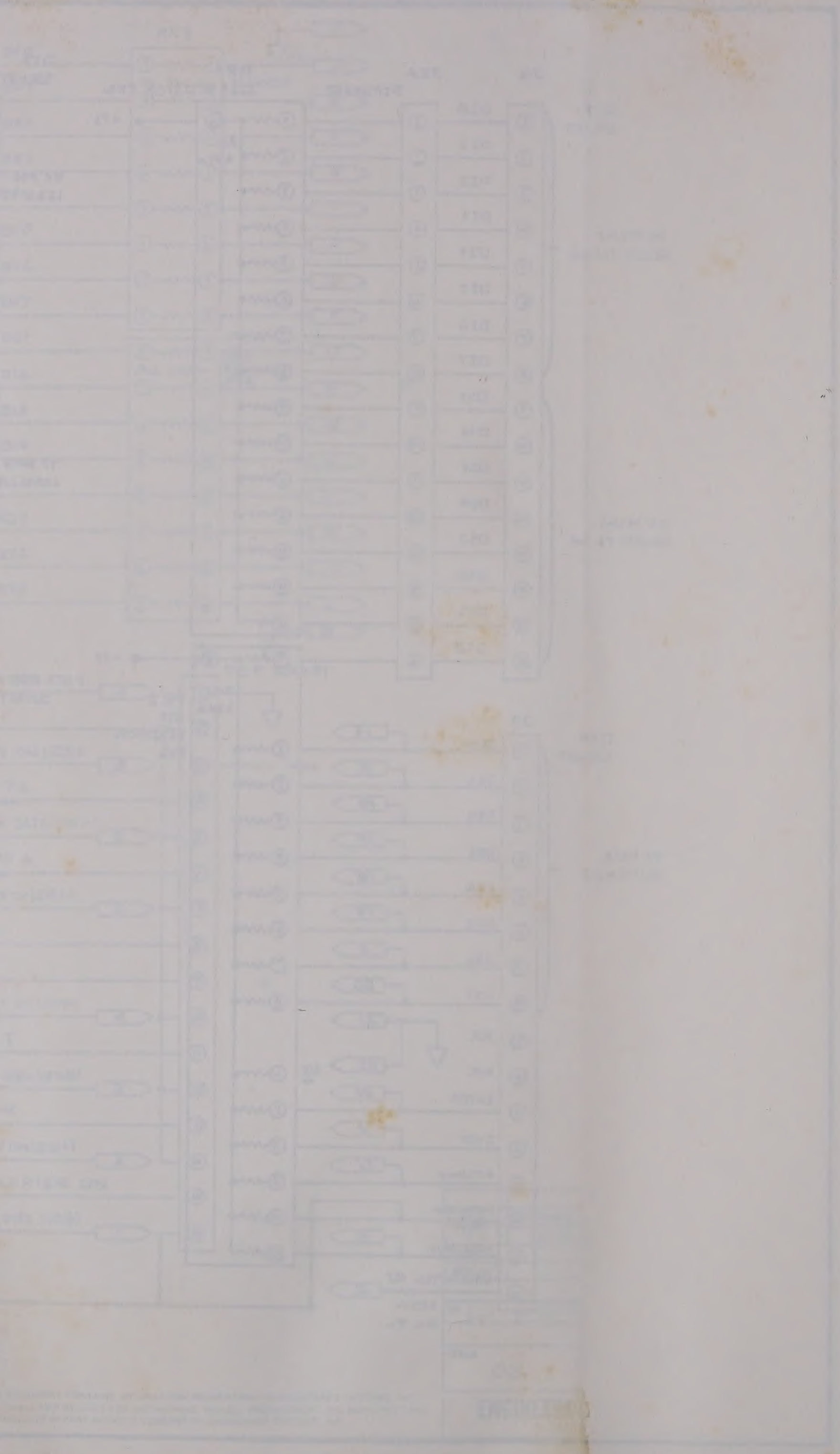
TITLE SCHEMATIC DIAGRAM - CENTRAL /REMOTE TEST SET PANEL INTERCONNECTION BOARD

ISSUE 02

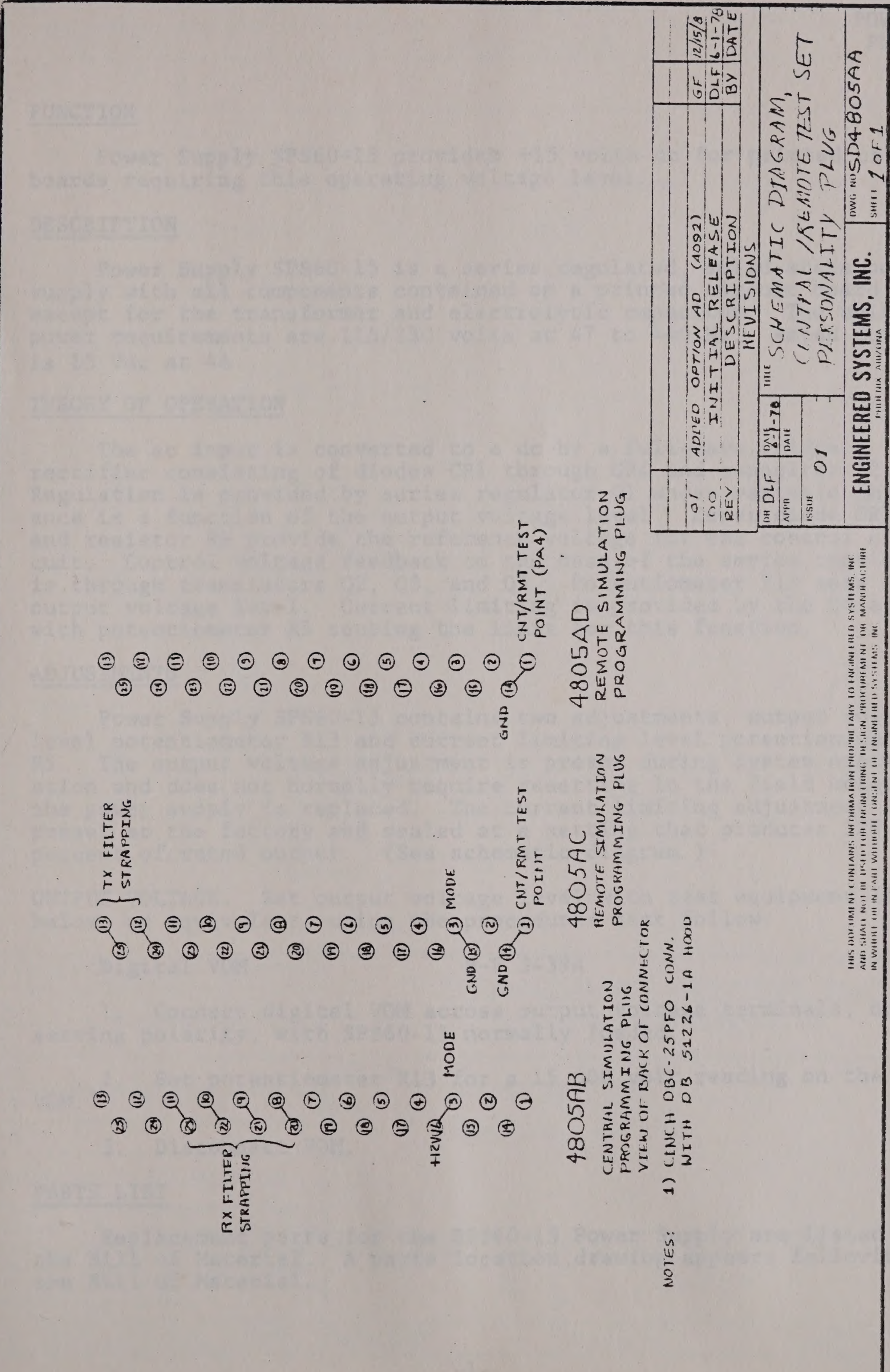
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO ENGINEERED SYSTEMS INC AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT CONSENT OF ENGINEERED SYSTEMS INC

ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA

DWG NO SD4158AA



BILL OF MATERIAL				NAME REMOTE PERSONALITY PLUG	NO. BM4805AD00
ITEM	QTY.	PART NO.	MFR.	DESCRIPTION	REFERENCE
1	1	DBC25PF0	CINCH	CONNECTOR, DATA PHONE	P2B
2	1	DB51226-1A	CINCH	HOOD, CONNECTOR	
3	AR	NPN	COML	WIRE, SOLID, #22 AWG	(NOTE 2)


RX FILTER STRAPPING
+12V
MODE
4805AB
CENTRAL SIMULATION PROGRAMMING PLUG
VIEW OF BACK OF CONNECTOR
TX FILTER STRAPPING
MODE
GND
GND
CNT/RMT TEST POINT
4805AC
REMOTE SIMULATION PROGRAMMING PLUG
GND
CNT/RMT TEST POINT (PA4)
4805AD
REMOTE SIMULATION PROGRAMMING PLUG
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
NOTES:
1) CINCH DBC-25PFO CONN. WITH DB 51226-1A HOOD
01 ADDED OPTION AD (A092) GF 12/15/8
00 INITIAL RELEASE DLF 6-1-78
REV DESCRIPTION BY DATE
REVISIONS
DR DLF DATE 6-1-78
APPR DATE
ISSUE 01
TITLE SCHEMATIC DIAGRAM, CENTRAL/REMOTE TEST SET PERSONALITY PLUG
ENGINEERED SYSTEMS, INC.
PHOENIX ARIZONA
DWG NO SD4805AA
SHEET 1 OF 1
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO ENGINEERED SYSTEMS, INC AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT CONSENT OF ENGINEERED SYSTEMS, INC.

FUNCTION

Power Supply SPS60-15 provides +15 volts dc for printed circuit boards requiring this operating voltage level.

DESCRIPTION

Power Supply SPS60-15 is a series regulated, solid-state power supply with all components contained on a printed circuit board, except for the transformer and electrolytic capacitor. The unit power requirements are 115/230 volts at 47 to 440 Hz. Rated output is 15 Vdc at 4A.

THEORY OF OPERATION

The ac input is converted to a dc by a full-wave bridge rectifier consisting of diodes CR1 through CR4 and capacitor C2. Regulation is provided by series regulator Q1 whose variable impedance is a function of the output voltage level. Zener diode CR5 and resistor R9 provide the reference voltage for the control circuit. Control voltage feedback to the base of the series regulator is through transistors Q2, Q3, and Q5. Potentiometer R13 sets the output voltage level. Current limiting is provided by the Q4 stage with potentiometer R5 setting the limit for this function.

ADJUSTMENTS

Power Supply SPS60-15 contains two adjustments; output voltage level potentiometer R13 and current limiting level potentiometer R5. The output voltage adjustment is preset during system optimization and does not normally require resetting in the field unless the power supply is replaced. The current limiting adjustment is preset at the factory and sealed at a setting that produces 120 percent of rated output. (See schematic diagram.)

OUTPUT VOLTAGE. Set output voltage level with test equipment listed below, or equivalent, using the procedures that follow:

Digital VOM	H-P 3439A

1. Connect digital VOM across output voltage terminals, observing polarity, with SPS60-15 normally loaded.

2. Set potentiometer R13 for a 15.000 volt reading on the VOM.

3. Disconnect VOM.

PARTS LIST

Replacement parts for the SPS60-15 Power Supply are listed in the Bill of Material. A parts location drawing appears following the Bill of Material.

REVISIONS

REV.	BY	DESCRIPTION	APPR.	DATE

```
          BILL OF MATERIALS. 01-102722-00 REV B   SPS 60-15     FIRST RELEASED: 11 NOV 74     11:35:16  22 NOV 1976

ITEM* PART#.......... REV QTY DESCRIPTION...................... REF-DES.................................. LAST-CHANGE..

  1  01-102722-00     B   REF SPS 60-15
  2  12-102723-00     B   REF SCHEM SPS 60-15
  3  04-101179-00     C     1 XFMR 60-15                        T1
  4  05-101040-00     K     1 CHASSIS SPS 60/75 (STD)
  5  02-102724-00     D     1 PWA REG 60-15
  6  03-103217-01     C     2 KIT DIODE MTG #10 STUD
  7
  8
  9
 10  06-109102-12     B     1 CAP 15KUF 30V                     C1
 11  09-109181-01     A     2 RECT 20A 100V 20F10               CR1,2
 12  08-109131-01     B     1 RES WWC 5W 10% .10                R1
 13  08-109116-68           1 RES CC 1/2W 5% 270                R2
 14  08-109116-82           1 RES CC 1/2W 5% 1000               R3
 15  09-109141-01     A     2 XSTR 2N3055                       Q1,2
 16
 17
 18
 19  10-109219-01           1 TERMINAL- INSUL S1T
 20  10-109227-02     A     1 BRKT CAP 3 LEG 2" 1782-02
 21  10-109239-01     A     2 SOCKET XSTR TO-3 8080-1G1
 22  10-109253-02           3 SPACER NYLON SP-33
 23  10-109271-01           2 INSULATOR XSTR (MICA) TO-3
 24  10-109300-02           3 RIVET 1601-0512
 25  10-109300-03           4 RIVET 1601-0613
 26  10-109301-01           3 RIVET BSP4-6
 27  10-109230-01          AR THERMAL COMPOUND
```

SIGNATURES	DATES
DWN.	
CHK.	
DSGN.	
ENGR.	
APPR.	

STANDARD POWER, INC.
SANTA ANA, CALIFORNIA 92705

TITLE
BILL OF MATERIAL
POWER SUPPLY

PROPRIETARY NOTICE

ALL PATENT OR OTHER PROPRIETARY RIGHTS PERTAINING TO THE ITEMS SOLD HEREUNDER SHALL REMAIN THE SOLE PROPERTY OF STANDARD POWER, INC. EXCEPT THAT THE PURCHASER SHALL HAVE THE RIGHT TO USE SUCH ITEMS FOR THEIR INTENDED PURPOSE.

CODE IDENT	SIZE	DWG. NO.	REV.
	A	SPS60-15	

DO NOT SCALE DWG.

SCALE:

WEIGHT:

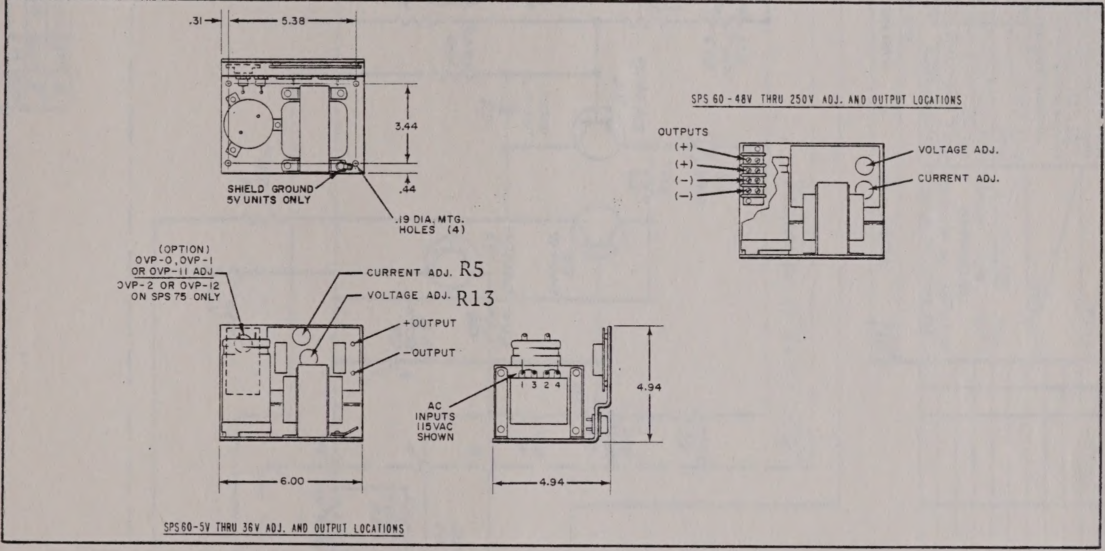
SHEET 1 OF 2

REVISIONS

REV.	BY	DESCRIPTION	APPR.	DATE

28
29
30
31 13-109312-37 4 SCREW PAN SLOT 6-32 9/16
32 13-109320-03 4 WASHER LK INT TOOTH #6
33 13-109320-05 1 WASHER LK INT TOOTH #10

3246*12435


.31
5.38
3.44
.44
SHIELD GROUND
5V UNITS ONLY
.19 DIA. MTG.
HOLES (4)
OUTPUTS
(+)
(+)
(−)
(−)
VOLTAGE ADJ.
CURRENT ADJ.
(OPTION)
OVP-0, OVP-1
OR OVP-11 ADJ
OVP-2 OR OVP-12
ON SPS 75 ONLY
CURRENT ADJ. R5
VOLTAGE ADJ. R13
+OUTPUT
−OUTPUT
AC
INPUTS
115VAC
SHOWN
1 3 2 4
4.94
6.00
4.94

SPS 60 - 48V THRU 250V ADJ. AND OUTPUT LOCATIONS

SPS60-5V THRU 36V ADJ. AND OUTPUT LOCATIONS

SIGNATURES	DATES
DWN.	
CHK.	
DSGN.	
ENGR.	
APPR.	

STANDARD POWER, INC.
SANTA ANA, CALIFORNIA 92705

TITLE
PARTS LOCATION DRAWING
POWER SUPPLY

PROPRIETARY NOTICE

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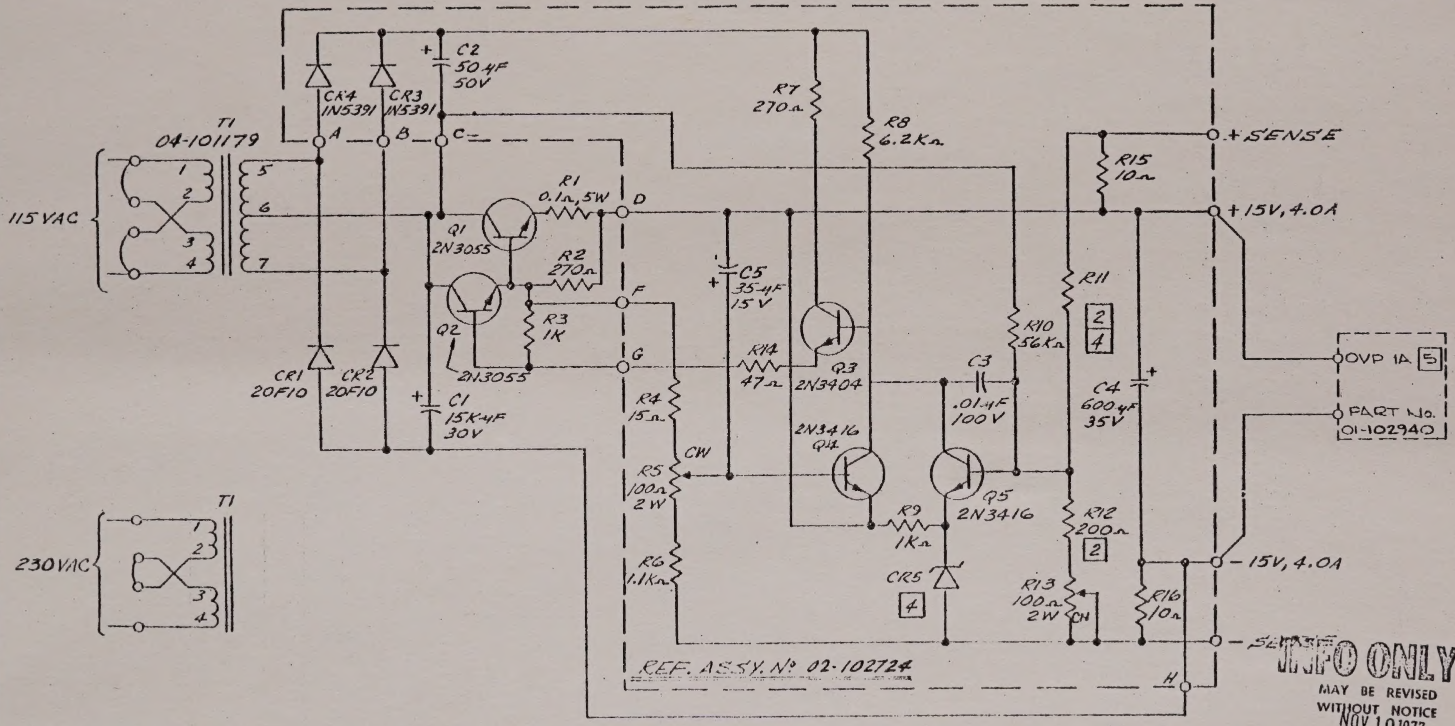
CODE IDENT	SIZE	DWG. NO.	REV.
	A	SPS60-15	

DO NOT SCALE DWG.

SCALE:	WEIGHT:	SHEET 2 OF 2

REV.	BY	DESCRIPTION	APPR	DATE
A	LTE	INITIAL RELEASE	—	—
B		INCORPORATED ECO 12006		


T1
04-101179
115 VAC
1
2
3
4
5
6
7
CR4
1N5391
CR3
1N5391
A
B
C
C2
50 μF
50V
CR1
20F10
CR2
20F10
C1
15K μF
30V
Q1
2N3055
Q2
2N3055
R1
0.1Ω, 5W
R2
270Ω
R3
1K
D
F
G
R4
15Ω
R5
100Ω
2W
CW
R6
1.1KΩ
C5
35 μF
15 V
R14
47Ω
Q3
2N3404
R7
270Ω
R8
6.2KΩ
2N3416
Q4
R9
1KΩ
CR5
4
C3
.01 μF
100 V
Q5
2N3416
R10
56KΩ
R11
2
4
R12
200Ω
2
R13
100Ω
2W
CH
C4
600 μF
35V
R15
10Ω
R16
10Ω
+ SENSE
+15V, 4.0A
−15V, 4.0A
− SENSE
H
OVP 1A
5
PART No.
01-102940
T1
230VAC
1
2
3
4
REF. ASSY. Nº 02-102724

INFO ONLY
MAY BE REVISED
WITHOUT NOTICE
NOV 10 1977

QTY REQ'D	DESCRIPTION	PART NO.	MATERIAL	MANUFACTURER	ITEM NO.

LIST OF MATERIAL

5 OVP OPTIONAL

4 SELECT 1N4735A, CR5 = 5.9 → 6.09V ; R11 = 330Ω
CR5 = 6.1 → 6.29V ; R11 = 300Ω
CR5 = 6.3 → 6.49V ; R11 = 270Ω

3. REFERENCE ASSEMBLIES 01-102722
02-102724

2 FILM RESISTOR, OHMS ± 2%, 1/2 W

1. CARBON RESISTORS, OHMS ± 5%, 1/2 W

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY.	USED ON
	60-15

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES

FRAC.	DEC.	ANGLES
±1/32	.XX ±.02 .XXX ±.010	±1/2°

MATERIAL:

FINISH:

SIGNATURES	DATES
DWN.	11-5-74
CHK.	11-3-74
DSGN.	11-3-74
ENGR.	
APPR.	11-3-74

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DO NOT SCALE DWG.

STANDARD POWER, INC.
Orange, California

TITLE
SCHEMATIC - POWER
SUPPLY, REMOTE SENSE
MODEL: SPS 60-15, 4.0A

CODE IDENT	SIZE	DWG. NO.	REV.
	C	12-102723	B

SCALE: —
WEIGHT: —
SHEET 1 OF 1